**UNITED STATES DISTRICT COURT**
**FOR THE EASTERN DISTRICT OF TEXAS**
**MARSHALL DIVISION**

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| **FAIRCHILD SEMICONDUCTOR CORPORATION, a Delaware corporation, and INTERSIL CORPORATION, a Delaware corporation,**<br><br>**Plaintiffs,**<br><br>**v.**<br><br>**POWER INTEGRATIONS, INC., a Delaware corporation,**<br><br>**Defendants.** | **C.A. No. 2-06CV-151 JTW** |

**POWER INTEGRATIONS' MOTION TO DISMISS OR, IN THE ALTERNATIVE, TO TRANSFER THIS CASE TO DELAWARE**

Fairchild does not have standing to prosecute this case because it does not own U.S. Patent No. 5,264,719 ("the '719 patent") and is not the exclusive licensee of the patent. Fairchild's recent efforts to buy a cause of action on the '719 patent from Intersil are insufficient as a matter of law, and no amount of hand-waving on the part of the plaintiffs can cure that fatal defect. Therefore, pursuant to Rule 12(b)(1) of the Federal Rules of Civil Procedure, Power Integrations hereby moves to dismiss this case for lack of standing.

In the alternative, Power Integrations asks that the Court transfer this action to the District of Delaware, where the parties are already engaged in a dispute regarding the '719 patent. Specifically, the parties are seeking to determine whether the '719 patent was conceived before a Power Integrations patent asserted in the Delaware action. The Delaware case is set for trial this year, and all parties in the present suit are involved in the Delaware matter—Power

Integrations is the Delaware plaintiff, Fairchild Semiconductor is the defendant, and Intersil is a third party alleging prior inventorship and working with Fairchild to attempt to prove prior inventorship. As a result, this District is not the proper venue in which to address the '719 patent.

## I. FACTUAL BACKGROUND

On October 20, 2004, Power Integrations, Inc. ("Power Integrations") filed suit against Fairchild Semiconductor Corporation and Fairchild Semiconductor International, Inc. (collectively "Fairchild") in the District Court for the District of Delaware, alleging infringement of four U.S. patents. [*See* Declaration of Mike Jones ("Jones Decl.") Ex. A.[1]] Fairchild claims that one of the four patents, U.S. Patent No. 4,811,075 ("the '075 patent"), is invalid in view of the '719 patent, the only patent asserted in this case. Fairchild and Power Integrations have taken extensive discovery with respect to the '719 patent in the Delaware action, and the dispute in Delaware turns on who was the first to invent the technology in the '075 and '719 patents. A Delaware jury will resolve this critical issue later this year, as the trial on validity issues is set to begin on December 4. [Ex. B (Pretrial Conference Tr.) at 30-31.]

During the course of the Delaware litigation, Fairchild bought a license "to enforce" the '719 patent against a single entity: Power Integrations. [*See* Fairchild's Amended Complaint ("Amended Complaint") Ex. E.] By the terms of the March 30, 2006 agreement, Intersil granted Fairchild "the sole and exclusive right . . . to assert, litigate and prosecute claims of [i]nfringement under the ['719] patent[] against [Power Integrations]." [Amended Complaint Ex. E (Patent License Agreement of Mar. 30, 2006 ("PLA")) at §§ 1.2, 3.1.] However, Fairchild's hunting license does not provide any underlying right beyond the right to sue—it

[1] All citations are to the accompanying Declaration of Mike Jones, unless noted otherwise.

does not grant Fairchild the exclusive right to make, use, or sell the alleged invention of the '719 patent.[2]

On April 11, 2006, Fairchild issued a press release announcing the license and the institution of this suit, noting that Fairchild "recently secured exclusive rights to assert the ['719] patent against Power Integrations." [Ex. C (April 11, 2006 Press Release – *Fairchild Semiconductor Files Patent Infringement Lawsuit Against Power Integrations, Inc.*).] On May 18, 2006, Intersil and Fairchild executed a Supplemental Agreement attempting to modify the PLA to make yet another entity, Intersil Americas, the original party to the PLA. [Amended Complaint Ex. F (Agreement of May 18, 2006).] None of these actions conferred standing on Fairchild.

## II. LEGAL AUTHORITY

To have standing to assert patent infringement, "the plaintiff must demonstrate that it held enforceable title to the patent at the inception of the lawsuit." *Paradise Creations, Inc. v. U V Sales, Inc*., 315 F.3d 1304, 1309 (Fed. Cir. 2003). Where the plaintiff lacks a cognizable injury at the time it filed suit, such defect in standing cannot be cured after the inception of the lawsuit. *Id.* at 1310. In order to bring an action for damages resulting from infringement, the patentee must not only have legal title to the patent, but must have been its owner at the time of the infringement. *Crown Die & Tool Co. v. Nye Tool & Machine Works*, 261 U.S. 24, 41 (1923); *Arachnid, Inc. v. Merit Indus., Inc*., 939 F.2d 1574, 1579 (Fed. Cir. 1991) ("[O]ne seeking to recover money damages for infringement of a United States patent . . . must have held the legal title to the patent during the time of the infringement."); *Heidelberg Harris, Inc. v. Loebach*, 145 F.3d 1454, 1458 (Fed. Cir. 1998) ("[A] plaintiff cannot sue for patent infringement occurring

[2] As part of a broader cross-license with Intersil, Fairchild took a license to practice the '719 patent in certain limited capacities several years ago. But that license is not exclusive and, as Fairchild has implicitly acknowledged by entering into at least two later agreements specific to the '719 and Power Integrations, has no bearing on the instant dispute. Plaintiffs have not asserted—and cannot assert—that the earlier Fairchild-Intersil license in any way confers standing in this case.

prior to the time the plaintiff actually obtained legal title to the asserted patent."); *Mas-Hamilton Group v. LaGard, Inc*., 156 F. 3d 1206, 1210 (Fed. Cir. 1998) (only the owner of the patent at the time of the infringement can bring an action for damages resulting from that infringement) (dictum).

A patentee may divide its "bundle of rights" and convey, or share, the right to sue infringers. The patentee may, by instrument in writing, assign, grant, convey (1) the entire patent, (2) an undivided part or share of the entire patent, or (3) all rights under the patent in a specified geographical region. *Waterman v. Mackenzie*, 138 U.S. 252, 255 (1891). Such transfers constitute an assignment, and they vest the assignee with title in the patent and a right to sue infringers, either as sole plaintiff or as co-plaintiff depending on the nature and extent of the rights conferred. *Id.* However, a transfer of less than one of these three interests is a mere license, giving the licensee no title in the patent, and no right to sue for infringement in the licensee's own name. *Id.* Fairchild has none of these three interests.

A narrow exception to the rule that only patentees and successors in interest may sue for infringement applies when a party obtains an exclusive license to a patent and holds "all substantial rights" under the patent. *See Textile Productions, Inc. v. Mead Corp*., 134 F.3d 1481, 1483-85 (Fed. Cir. 1998); *Vaupel Textilmaschinen KG v. Meccanica Euro Italia S.P.A.*, 944 F.2d 870, 875 (Fed. Cir. 1991). To establish independent standing as an exclusive licensee, though, a party must have received both the right to exclude others from making, using, or selling the patented technology and the patent holder's promise that no other party may practice the patented technology. *Rite-Hite Corp. v. Kelley Co*., 56 F.3d 1538, 1552 (Fed. Cir. 1995).

However, this narrow exception does not apply to non-exclusive licensees; even if the patent holder is a party to the suit, a non-exclusive licensee does not have independent standing to sue for infringement. *Kalman v. Berlyn Corp*., 914 F.2d 1473, 1481-82 (Fed. Cir. 1990)

(stating a non-exclusive licensee lacks standing to sue for infringement even if joined with the patent holder and further noting that no "licensee who joins the patentee [has] standing to sue an infringer"). Furthermore, a non-exclusive licensee who has not been granted the right to exclude others has no legally recognized interest that would entitle it to bring or join an infringement action. *Abbott Lab. v. Diamedix Corp.*, 47 F.3d 1128, 1131 (Fed. Cir. 1995). A licensee may only bring an infringement suit to protect a property interest it received from the patentee. *See Ortho Pharmaceutical Corp. v. Genetics Institute, Inc.*, 52 F.3d 1026, 1034 (1995) ("[I]t is the licensee's beneficial ownership of a right to prevent others from making, using, or selling the patented technology that provides the foundation for co-plaintiff standing."). Thus, a contract clause cannot by itself grant standing to a licensee if the licensee would otherwise not have standing to bring the suit. *Id.* ("[A] right to sue clause cannot negate the requirement that . . . a licensee must have beneficial ownership of some of the patentee's proprietary rights.").

## III. ARGUMENT

### A. Fairchild Does Not Have Standing and Cannot Sue Power Integrations on the '719 Patent.

Fairchild has no standing to sue for infringement because Fairchild is not, and never was, the patentee or successor in interest to the '719 patent, and at no time has Fairchild held all substantial rights to the patent. Patent standing rules are strict: a party seeking to recover for alleged patent infringement must either have held legal title to the patent at the time of the alleged infringement, or have been assigned the right to recover for that infringement by the legal title holder together with an assignment of all substantial rights under the patent. *Crown Die & Tool Co.*, 261 U.S. at 41; *Ortho Pharm.*, 52 F.3d at 1034. Only a patentee may bring an action for patent infringement, and Fairchild is not the patentee. Legal title appears to have been held at all times by Intersil (or Intersil's predecessor Harris Corporation), making Intersil the only party

with any right to recover for alleged patent infringement, regardless of Fairchild's purported "license to enforce" the patent against Power Integrations.

To overcome the rule that only patentees and successors in interest may sue for infringement, Fairchild would need an exclusive license and would need to demonstrate a sufficient proprietary injury to one of the rights that flows from the patent. *Rite-Hite*, 56 F.3d at 1552. In essence, though, Fairchild has a "bare license," because it has no exclusive right to keep others from making, using, or selling products making use of the patented technology, and Fairchild suffers no legally cognizable harm when a third-party makes, uses, or sells the patented technology. *See Abbott*, 47 F.3d at 1131. As noted above, a bare licensee has no standing at all. *See Rite-Hite*, 56 F.3d at 1552; *Ortho Pharm.*, 52 F.3d at 1034. Fairchild therefore has no legally recognized interest that entitles it to bring or join an infringement action.

Intersil's contractual grant of the "exclusive right to sue" is not sufficient to confer standing to Fairchild. "A patentee may not give a right to sue to a party who has no proprietary interest in the patent." *Ortho Pharm.*, 52 F.3d at 1034 (collecting cases describing non-exclusive licensees lack standing to enforce a patent); *Rite-Hite*, 56 F.3d at 1553. *See also Phila. Brief Case Co. v. Specialty Leather Prods. Co*., 145 F. Supp. 425, 429-30 (D.N.J. 1956*), aff'd*, 242 F.2d 511 (3rd Cir. 1957) (contract clause cannot give right to sue where licensee would otherwise have no such right). The Patent License Agreement attempts to convey to Fairchild "the sole and exclusive right . . . to assert, litigate and prosecute claims of [i]nfringement under the ['719 and related] patents against [Power Integrations]" [Amended Complaint Ex. E (Patent License Agreement of Mar. 30, 2006) at §§ 1.2, 3.1], but the license agreement simply cannot supersede the legal requirement that the licensee have all substantial rights in order to have standing to sue for infringement.

The Federal Circuit has explicitly rejected the possibility that a patentee could grant a hunting license along the lines of the license contemplated between Fairchild and Intersil. *See Prima Tek II, LLC v. A-Roo Co.*, 222 F.3d 1372, 1381 (Fed. Cir. 2000). The court in *Prima Tek II* further noted that "[i]n evaluating whether a particular license agreement transfers all substantial rights in a patent to the licensee, we pay particular attention to whether the agreement conveys *in full* the right to exclude others from making, using and selling the patented invention in the exclusive territory." *Id.* at 1379 (emphasis in original, citations omitted). Just last month, the Federal Circuit affirmed these principals:

> [T]he plaintiff must be within the class of persons legally protected by the statute under which the individual seeks relief. For example, in *Ortho Pharmaceutical Corp. v. Genetics Institute, Inc.*, 52 F.3d 1026, 1030-31 (Fed.Cir.1995), we held that nonexclusive patent licensees lack Article III standing to sue for infringement because "economic injury alone does not provide standing to sue under the patent statute . . . . a licensee must hold some of the proprietary sticks from the bundle of patent rights," otherwise the licensee "suffers no legal injury from infringement and, thus, has no standing . . . ." *See also Intellectual Prop. Dev., Inc. v. TCI Cablevision of Cal., Inc.*, 248 F.3d 1333, 1345 (Fed.Cir.2001) ("[A] nonexclusive license . . . confers no constitutional standing on the licensee under the Patent Act to bring suit or even to join a suit with the patentee because a nonexclusive (or 'bare') licensee suffers no legal injury from infringement.").

*Willis v. Government Accountability Office*, --- F.3d ----, 2006 WL 1329929 (Fed. Cir. May 17, 2006). The Court should therefore decline to expend its resources on Fairchild's ill-conceived distraction from the Delaware case.

Moreover, Intersil's presence in this suit does not overcome Fairchild's lack of independent standing. Adding the patent holder as a co-plaintiff would only defeat a challenge on the grounds of standing if Fairchild had the exclusive rights to make, use and sell the patented technology, *Abbott*, 47 F.3d at 1131, but as Fairchild does not have such exclusive rights, it lacks standing to bring a cause of action for infringement. The Court should therefore dismiss this action for lack of standing.

**B. If the Court Does Not Dismiss This Action, It Should Transfer the Case to Delaware to Be Resolved In The Court Which is Already Addressing the Patent-in-Suit.**

In the alternative, Power Integrations asks the Court to transfer this action to the United States District Court for the District of Delaware, where a previously filed case involving the same parties and an identical dispute regarding who was first to invent the technology is already pending. There is a substantial overlap between this action and the Delaware case set for trial this December, as the outcome of both suits depends on the Delaware case's inventorship findings, and both the Fifth Circuit and the Federal Circuit both follow a first-to-file rule for cases having substantial overlap. Further, the interest of justice suggests transfer under the federal venue statute. Therefore, if the Court does not dismiss this case outright, it should transfer to the matter to Delaware.

**1. The Key Issue With Respect to the Sole Patent-in-Suit, an Inventorship Dispute, is Already Before the Delaware Court.**

In support of its invalidity claim with respect to the '075 patent in Delaware, Fairchild asserted that the '719 patent, the only patent in this case, is key invalidating prior art to the '075 patent. [Ex. D ('719 patent claim chart from Fairchild's invalidity contentions).] Fairchild and Power Integrations have taken extensive discovery with respect to the '719 patent, and the dispute in Delaware turns on who was the first to invent the technology in the '075 and '719 patents. The Delaware jury will resolve this critical issue later this year.

The '719 Patent was filed on May 24, 1991, over four years after the '075 Patent's April 1987 filing date. During prosecution of the '719 patent, the Applicant copied large portions of the claims of the '075 patent into the '719 patent. [Ex. E at I-000228 ("[A]lthough not identically copied, [the claim] is considered to be generic to the invention defined in claim 1 of U.S. Patent No. 4,811,075 to Eklund." (underlining in original)).] A brief comparison of claim 8

of the '719 Patent to claim 1 of the '075 Patent demonstrates this copying of the '075 patent claim language. [Appendix 1; Ex. F-G.] Thus, the same questions regarding conception and inventorship that are central to the Delaware trial would also arise in this suit.

**2. The First-To-File Rule Compels the Transfer of This Case.**

In patent cases, "the forum of the first-filed case is favored, unless considerations of judicial and litigant economy, and the just and effective disposition of disputes, require otherwise." *Genentech, Inc. v. Eli Lilly & Co.*, 998 F.2d 931, 937 (Fed. Cir. 1993), *overruled on other grounds*, *Wilton v. Seven Falls, Inc.*, 515 U.S. 277 (1995); *accord Save Power Ltd. v. Syntek Finance Corp.*, 121 F.3d 947, 950 (5th Cir. 1997) ("The Fifth Circuit adheres to the general rule that the court in which an action is first filed is the appropriate court to determine whether subsequently filed cases involving substantially similar issues should proceed.") The Federal Circuit regards the application of the first-to-file rule as an issue that "is important to national uniformity in patent practice." *Genentech*, 998 F.2d at 937. Application of the rule requires a three-part analysis by the court in a later-filed action:

1. The court must confirm that the case before it was filed later than an earlier case in another district. *Genentech*, 998 F.2d at 937; *accord Syntek Finance*, 121 F.3d at 950-51.

2. The court must then determine whether the earlier-filed case is likely to raise issues that substantially overlap with the case on its own docket. *Syntek Finance*, 121 F.3d at 950-51.

3. If so, the court must transfer the action before it to the first-filed court unless it finds that it would be "unjust or inefficient" to do so. *Genentech*, 998 F.2d at 938; *accord Mann Mfg., Inc. v. Hortex, Inc.,* 439 F.2d 403 (5th Cir. 1971) (transfer required absent "compelling" reasons to favor later action).

After the second case is transferred, the first-filed court decides whether that later action "must be dismissed, stayed, or transferred and consolidated." *Sutter Corp. v. P&P Indus., Inc.*, 125

F.3d 914, 920 (5th Cir. 1997). In favoring transfer of related cases, the rule is designed to avoid the waste and duplication that would result from piecemeal resolution of similar issues. *West Gulf Maritime Assoc. v. ILA Deep Sea Local 24*, 751 F.2d 721, 728-29 (5th Cir. 1985); *cf. Optical Recording Corp. v. Capitol-EMI Music, Inc.*, 803 F. Supp. 971 (D. Del. 1992) (proceeding with later-filed case because the Delaware court was already familiar with the technology and patents at issue in both cases).

**a. The Delaware Action Is The First-Filed Action.**

Power Integrations filed suit against Fairchild on October 20, 2004, in Delaware, over 17 months before the current action was brought. Fairchild has not only answered the complaint in the Delaware case, but the parties have already conducted extensive discovery, are finished with claim construction, and have completed technical expert discovery. In fact, the parties recently had a pre-trial conference, and the Delaware Court provided trial dates for later this year (September for some issues and December for others). [Ex. B at 30-31.]

**b. There Is Substantial Overlap in the Subject Matter of the Patents at Issue.**

Cases do not need to have exactly the same subject matter to meet the "substantial overlap" test. "[R]egardless of whether or not the suits here are identical, if they overlap on the substantive issues, the cases would be required to be consolidated in . . . the jurisdiction first seized of the issues." *Mann Mfg.*, 439 F.2d at 408 n.6; *see also Syntek Finance*, 121 F.3d at 950 ("The rule does not, however, require that cases be identical.")

The Fifth Circuit has addressed the meaning of "substantial overlap" in the context of patent litigation in *Mann Mfg.* 439 F.2d at 405-408. There, Goodrich sued in the Southern District of New York seeking a declaratory judgment that a number of its products did not infringe a patent owned by Mann. *Id.* at 405. After Goodrich commenced that action, Mann

sued Goodrich and Hortex on the same patent in the Western District of Texas and then sued on another related patent. *Id.* at 405-406. The Fifth Circuit acknowledged that these two cases involved distinct patents, but despite the difference in patent claims, the Court found that the cases shared substantial issues and held that the New York court was the proper court to determine how to proceed with respect to the later added patent. *Id.* at 407-08.

Here, the Delaware and Texas cases bear even more similarities than in *Mann Mfg.*, as both cases address the same technology and share disputes regarding nearly identical claims. The similarity is particularly evident when comparing claim 8 from the'719 Patent against claim 1 of the '075 Patent (shown side-by-side in Appendix 1). The parties have taken extensive fact and expert discovery on the question of inventorship in the Delaware case, and the Delaware Court has already issued a claim construction order. [Ex. H (Claim Construction Order).] The identical question of inventorship, likely determinative for validity purposes, will be decided at trial in Delaware later this year on the basis of the same fact witnesses, documents, and expert testimony that would apply here. As such, to proceed with both the Texas and Delaware cases separately would result in precisely the kind of wasteful duplication of time and effort that the first-to-file rule is designed to prevent. *West Gulf*, 751 F.2d at 729 ("The concern manifestly is to avoid the waste of duplication . . . and to avoid piecemeal resolution of issues that call for a uniform result."). Allowing this case to proceed in Texas would also risk conflicting outcomes on a single issue. To avoid this confusion and injustice, Power Integrations asks this Court to transfer the action to Delaware.

**c. There Are No Compelling Circumstances That Justify Disregarding the First-To-File Rule.**

Once the first-to-file rule applies, the issues should be decided in the first-filed suit, unless it would be "unjust or inefficient" to do so. *Genentech*, 998 F.2d at 938. In deciding

whether justice and efficiency require disregarding the first-to-file rule, the Federal Circuit considers such factors as: (1) the convenience and availability of witnesses, (2) the absence of jurisdiction over all parties, (3) the possibility of consolidation with related litigation, and (4) whether the first-filed case involves the real parties in interest. As discussed below, none of these factors weighs against transfer to Delaware.

First, the convenience and availability of witnesses do not favor the Eastern District of Texas. All three parties in this case are Delaware corporations, with their principal places of business alleged to be in either California or Maine. All of the patents in question, including those from the Delaware case, list the inventors' residence as either California or Florida. In fact, Power Integrations is not aware of a single fact witness located in the state of Texas.

Second, there are no jurisdictional reasons to disregard the first-to-file rule. Not only are Fairchild and Intersil Delaware corporations, but Fairchild also answered and counterclaimed in the Delaware case without asserting a defense based on a lack of personal jurisdiction or on the inconvenience of that forum. As such, Fairchild has agreed to jurisdiction and waived any right to object. *See Golden v. Cox Furniture Mfg. Co., Inc.*, 683 F.2d 115, 118 (5th Cir. 1982) (party waives right to object to personal jurisdiction if it does not make motion under Rule 12 or assert defense in answer); *see also* Fed. R. Civ. P. 12(h)(1). Intersil responded to subpoenas in the Delaware case and, as a Delaware corporation, cannot contest personal jurisdiction in Delaware.

The third factor also provides no basis for declining this transfer request, as there is no related litigation in the Eastern District of Texas with which the two actions could be consolidated. In fact, the opposite is true. As to the fourth factor, whether the first-filed case involves the real parties in interest, defendants will likely argue that Intersil is not a party to the Delaware action. However, Intersil has been working with Fairchild in Delaware case, shares

local counsel with Fairchild in Delaware, and has produced documents and things related to the '719 patent in Delaware. Intersil has also participated in and paid the inventor of the '719 patent to sit for a deposition, in addition to preparing and presenting alleged corroborating witnesses on the '719 patent. As such, Intersil has been an active participant in the Delaware litigation and is well aware that the inventorship contest between the '075 patent and the '719 patent will be decided in the Delaware case.

**3. The Interest of Justice Requires Hearing this Action in Delaware.**

Even if this Court does not transfer using the first-to-file rule, it should transfer the case to the District of Delaware because it is a more convenient and cost effective place to resolve the instant dispute. The potential for inconsistent rulings from the plaintiffs' forum shopping imposes significant inconvenience on Power Integrations, and to the public at large, in the form of uncertainty. Further, having presided over the Delaware case, the Delaware court will be intimately familiar with the technology and issues in the present suit, including specifically the inventorship contest, which plaintiffs apparently want to challenge all over again here. In addition, the need to re-litigate the inventorship contest imposes an inconvenience and burden on Power Integrations.

**a. Cases Are Transferred at the Court's Discretion, Focusing on Convenience and Justice.**

A district court may transfer any civil case "[f]or the convenience of parties and witnesses, in the interest of justice, . . . to any other district or division where it might have been brought." 28 U.S.C. § 1404(a). In exercising its discretion to transfer a pending case, courts consider "all relevant factors to determine whether or not on balance the litigation would more conveniently proceed and the interests of justice be better served by transfer to a different

forum." *Peteet v. Dow Chemical Co.*, 868 F.2d 1428, 1436 (5th Cir. 1989) (internal quotations and citations omitted).

**b. Both Convenience and Justice Favor Transfer to Delaware.**

The potential for inconsistent findings imposes a great inconvenience on Power Integrations and burdens the public at large. The Delaware case will proceed to judgment first, and that judgment is res judicata. Because the parties can rely on the Delaware court's findings, in particular the determination on the inventorship issue, all preparations made meanwhile to re-litigate the issues in this District would be wasted. Absent such consistent treatment, it could take years to untangle the various issues presented with multiple constructions and inventorship contentions on these related patents. Indeed, given the stage of the Delaware case, it is likely that issues from that case would be pending on appeal at the same time that plaintiffs ask this Court to decide those same issues. The public would have no idea what it could and could not do in this field.

Moreover, plaintiffs have known for over a year that inventorship would be decided in the Delaware case, and they could have filed a counterclaim asserting the '719 patent against Power Integrations early in the Delaware case. Instead, they chose to wait until the Delaware case was nearly completed, and then filed this suit in another forum, despite the fact that rulings and findings from the Delaware case are important, and in some cases determinative, in their present suit.

Finally, having presided over the Delaware case, the District of Delaware will be intimately familiar with the technology and issues in the present suit, including specifically claim constructions and the inventorship contest. The Delaware court will also be in the best position to decide evidentiary issues such as what evidence, rulings, and stipulations from the old case

may be employed in what ways in the present suit. This Court should therefore transfer the instant case to Delaware under Section 1404(a), to the extent it does not do so under the first-filed rule or does not dismiss the suit outright for lack of standing.

## III. CONCLUSION

For the reasons stated above, this Court should grant Power Integrations' motion to dismiss for lack of standing or, in the alternative, transfer the case to Delaware to be resolved by a Court already dealing with the '719 patent and familiar with the technology at issue in both cases.

Dated: June 19, 2006

Respectfully submitted,

By: */s/ Michael E. Jones*
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**CERTIFICATE OF SERVICE**

The undersigned hereby certifies that all counsel of record who are deemed to have consented to electronic service are being served with a copy of this document via the Court's CM/ECF system per Local Rule CV-5(a)(3) on June 19, 2006. Any other counsel of record will be served by facsimile transmission and first class mail.

*/s/ Michael E. Jones*
Michael E. Jones

**UNITED STATES DISTRICT COURT**
**FOR THE EASTERN DISTRICT OF TEXAS**

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| FAIRCHILD SEMICONDUCTOR CORPORATION, a Delaware corporation, INTERSIL AMERICAS, INC., a Delaware corporation and INTERSIL CORPORATION, a Delaware corporation<br>Plaintiffs,<br><br>v.<br><br>POWER INTEGRATIONS, INC., a Delaware corporation.<br>Defendant | § | 2:06cv-151 (TJW) |

**DECLARATION OF MICHAEL E. JONES IN SUPPORT OF POWER INTEGRATIONS, INC.'S MOTION TO DISMISS, OR IN THER ALTERNATIVE, TO TRANSFER THIS CASE TO DELAWARE**

I, Michael E. Jones, declare same based upon information and belief:

1. I am a shareholder at Potter Minton PC in Tyler, Texas. I am one of the attorneys representing defendant Power Integrations, Inc. in the above-captioned matter filed by Plaintiffs Fairchild Semiconductor Corporation ("Fairchild"), Intersil Americas, Inc. and Intersil Corporation ("Intersil").

2. Attached hereto as Exhibit "A" is a true and correct copy of the First Amended Complaint for Patent Infringement filed by Power Integrations against Fairchild Semiconductor Corporation and Fairchild Semiconductor International, Inc. in the United States District Court for the District of Delaware on June 30, 2005 ("the Delaware Lawsuit").

3. I am informed and believe that attached hereto as Exhibit "B" is a true and correct copy of the transcript of the Pretrial Conference held on May 31, 2006 in the Delaware Lawsuit.

4. I am informed and believe that attached hereto as Exhibit "C" is a true and correct copy of Fairchild's press release dated April 11, 2006.

5. I am informed and believe that attached hereto as Exhibit "D" is a true and correct copy of a claim chart regarding the '719 patent asserted in this case which is part of Fairchild's invalidity contentions in the Delaware case as set forth in its Supplemental Responses to Power Integrations' First Set of Interrogatories, dated June 30, 2005.

6. I am informed and believe that attached hereto as Exhibit "E" is a true and correct copy of an excerpt from the '719 file history concerning the '075 patent claim language.

7. I am informed and believe that attached hereto as Exhibit "F" is a true and correct copy of the '719 Patent.

8. I am informed and believe that attached hereto as Exhibit "G" is a true and correct copy of the '075 Patent.

9. I am informed and believe that attached hereto as Exhibit "H" is a true and correct copy of Claim Construction Order issued on March 31, 2006 in the Delaware Lawsuit.

I declare under penalty of perjury that the foregoing is true and correct to the best of my information and belief.

Signed: June 19, 2006

Michael E. Jones

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

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| POWER INTEGRATIONS, INC., a Delaware corporation,<br><br>Plaintiff,<br><br>v.<br><br>FAIRCHILD SEMICONDUCTOR INTERNATIONAL, INC., a Delaware corporation, and FAIRCHILD SEMICONDUCTOR CORPORATION, a Delaware corporation<br><br>Defendants. | **C.A. No. 047-1371-JJF**<br><br>**JURY TRIAL REQUESTED** |

**FIRST AMENDED COMPLAINT FOR PATENT INFRINGEMENT**

Plaintiff Power Integrations, Inc. hereby alleges as follows:

**THE PARTIES**

1. Power Integrations, Inc. ("Power Integrations") is incorporated under the laws of the state of Delaware, and has a regular and established place of business at 5245 Hellyer Avenue, San Jose, California, 95138.

2. Upon information and belief, defendant Fairchild Semiconductor International, Inc. is incorporated under the laws of the state of Delaware, with its headquarters located at 82 Running Hill Road, South Portland, Maine, 04106. Upon information and belief, defendant Fairchild Semiconductor Corporation is incorporated under the laws of the state of Delaware, with its headquarters located at 82 Running Hill Road, South Portland, Maine, 04106. (Fairchild Semiconductor International, Inc. and Fairchild Semiconductor Corporation hereinafter collectively "Fairchild Semiconductor.")

## JURISIDICTION AND VENUE

3. This action arises under the patent laws of the United States, Title 35 U.S.C. § 1 *et seq*. This Court has subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).

4. Upon information and belief, this Court has personal jurisdiction over defendants because defendants are incorporated, doing business and advertising in this judicial District.

5. Upon information and belief, venue is proper in this Court pursuant to 28 U.S.C. §§ 1391(b), (c) and 1400 because the defendants are subject to personal jurisdiction in this judicial District.

## GENERAL ALLEGATIONS

6. Power Integrations' products include its integrated pulse width modulation ("PWM") integrated circuits that are used in power supplies for electronic devices such as cellular telephones, LCD monitors and computers. These products are sold throughout the United States, including Delaware.

7. Upon information and belief, defendants manufacture PWM integrated circuits devices (e.g., devices intended for use in power conversion applications such as LCD monitor power supplies or battery chargers for portable electronics), and directly and through their affiliates, uses, imports, sells, and offers to sell the same throughout the United States, including Delaware.

## FIRST CAUSE OF ACTION

### INFRINGEMENT OF U.S. PATENT NO. 6,107,851

8. The allegations of paragraphs 1-7 are incorporated as though fully set forth herein.

9. Power Integrations is now, and has been since its issuance, the assignee and sole owner of all right, title, and interest in United States Patent No. 6,107,851, entitled "Offline Converter with Integrated Softstart and Frequency Jitter" ("the '851

patent"), which was duly and legally issued on August 22, 2000. A true and correct copy of the '851 patent is attached hereto as Exhibit A.

10. Upon information and belief, defendants have been and are now infringing, inducing infringement, and contributing to the infringement of the '851 patent by making, using, importing, selling, and offering to sell devices, including PWM integrated circuit devices, and/or inducing or contributing to the importation, use, offer for sale and sale by others of such devices covered by one or more claims of the '851 patent, all to the injury of Power Integrations.

11. Defendants' acts of infringement have injured and damaged Power Integrations.

12. Defendants' infringement has caused irreparable injury to Power Integrations and will continue to cause irreparable injury until defendants are enjoined from further infringement by this Court.

13. Upon information and belief, Defendants' infringement has been, and continues to be, willful so as to warrant enhancement of damages awarded as a result of its infringement.

**SECOND CAUSE OF ACTION**

**INFRINGEMENT OF U.S. PATENT NO. 6,249,876**

14. The allegations of paragraphs 1-7 are incorporated as though fully set forth herein.

15. Power Integrations is now, and has been since its issuance, the assignee and sole owner of all right, title, and interest in United States Patent No. 6,249,876, entitled "Frequency Jittering Control for Varying the Switching Frequency of a Power Supply" ("the '876 patent"), which was duly and legally issued on June 19, 2001. A true and correct copy of the '876 patent is attached hereto as Exhibit B.

16. Upon information and belief, defendants have been and are now infringing, inducing infringement, and contributing to the infringement of the '876 patent

by making, using, importing, selling, and offering to sell devices, including PWM integrated circuit devices and/or inducing or contributing to the importation, use, offer for sale and sale by others of such devices covered by one or more claims of the '876 patent, all to the injury of Power Integrations.

17. Defendants' acts of infringement have injured and damaged Power Integrations.

18. Defendants' infringement has caused irreparable injury to Power Integrations and will continue to cause irreparable injury until defendants are enjoined from further infringement by this Court.

19. Upon information and belief, Defendants' infringement has been, and continues to be, willful so as to warrant enhancement of damages awarded as a result of its infringement.

**THIRD CAUSE OF ACTION**

**INFRINGEMENT OF U.S. PATENT NO. 6,229,366**

20. The allegations of paragraphs 1-7 are incorporated as though fully set forth herein.

21. Power Integrations is now, and has been since its issuance, the assignee and sole owner of all right, title, and interest in United States Patent No. 6,229,366, entitled "Off-Line Converter with Integrated Softstart and Frequency Jitter" ("the '366 patent"), which was duly and legally issued on May 8, 2001. A true and correct copy of the '366 patent is attached hereto as Exhibit C.

22. Upon information and belief, defendants have been and are now infringing, inducing infringement, and contributing to the infringement of the '366 patent by making, using, importing, selling, and offering to sell devices, including PWM integrated circuit devices and/or inducing or contributing to the importation, use, offer for

sale and sale by others of such devices covered by one or more claims of the '366 patent, all to the injury of Power Integrations.

23. Defendants' acts of infringement have injured and damaged Power Integrations.

24. Defendants' infringement has caused irreparable injury to Power Integrations and will continue to cause irreparable injury until defendants are enjoined from further infringement by this Court.

25. Upon information and belief, Defendants' infringement has been, and continues to be, willful so as to warrant enhancement of damages awarded as a result of its infringement.

**FOURTH CAUSE OF ACTION**

**INFRINGEMENT OF U.S. PATENT NO. 4,811,075**

26. The allegations of paragraphs 1-7 are incorporated as though fully set forth herein.

27. Power Integrations is now, and has been since its issuance, the assignee and sole owner of all right, title, and interest in United States Patent No. 4,811,075, entitled "High Voltage MOS Transistors" ("the '075 patent"), which was duly and legally issued on March 7, 1989. A true and correct copy of the '075 patent is attached hereto as Exhibit D.

28. Upon information and belief, defendants have been and are now infringing, inducing infringement, and contributing to the infringement of the '075 patent by making, using, importing, selling, and offering to sell devices, including PWM integrated circuit devices and/or inducing or contributing to the importation, use, offer for sale and sale by others of such devices covered by one or more claims of the '075 patent, all to the injury of Power Integrations.

29. Defendants' acts of infringement have injured and damaged Power Integrations.

30. Defendants' infringement has caused irreparable injury to Power Integrations and will continue to cause irreparable injury until defendants are enjoined from further infringement by this Court.

31. Upon information and belief, Defendants' infringement has been, and continues to be, willful so as to warrant enhancement of damages awarded as a result of its infringement.

**PRAYER FOR RELIEF**

WHEREFORE, Plaintiff requests the following relief:

(a) judgment against defendants as to willful infringement of the '851 patent;

(b) judgment against defendants as to willful infringement of the '876 patent;

(c) judgment against defendants as to willful infringement of the '366 patent;

(d) judgment against defendants as to willful infringement of the '075 patent;

(e) a permanent injunction preventing defendants and their officers, directors, agents, servants, employees, attorneys, licensees, successors, assigns, and customers, and those in active concert or participation with any of them, from making, using, importing, offering to sell or selling any devices that infringe any claim of the '851, '876, '366, or '075 patents;

(f) judgment against defendants for money damages sustained as a result of defendants' infringement of the '851, '876, '366, and '075 patents;

(g) that any such money judgment be trebled as a result of the willful nature of Defendants' infringement;

(h) costs and reasonable attorneys' fees incurred in connection with this action pursuant to 35 U.S.C § 285; and

(i) such other and further relief as this Court finds just and proper.

**JURY DEMAND**

Plaintiff requests trial by jury.

Dated: June 30, 2005

FISH & RICHARDSON P.C.

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*Power Intergrations, Inc. v.*
*Fairchild Semiconductor International, Inc.*

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*Hearing*
*May 31, 2006*

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IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE
POWER INTEGRATIONS, INC., )
Plaintiff, )
v. )
FAIRCHILD SEMICONDUCTOR )
INTERNATIONAL, INC, and )
FAIRCHILD SEMICONDUCTOR )
CORPORATION, )
Defendants. )
United States District Court
844 King Street
Wilmington, Delaware
Wednesday, May 31, 2006
12:30 p.m.
BEFORE: THE HONORABLE JOSEPH J. FARNAN, JR.
United States District Court Judge
APPEARANCES:
SEAN P. HAYES, ESQ.
FRANK SCHERKENBACH, ESQ.
MICHAEL HEADLEY, ESQ.
FISH & RICHARDSON
For Power Integrations
G. HOPKINS GUY, ESQ
ORRICLE, HERRINGTON
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3 1 THE COURT: Be seated, please.

[2] Good afternoon.

[3] (All respond: "Good afternoon.")

[4] **THE COURT:** I've reviewed the [5] proposed pretrial order, and this afternoon [6] I'll be entering an order that essentially [7] denies the motions for summary judgment and [8] also grants partial summary judgment to [9] Fairchild with regard to the damages evidence.

[10] If there's any questions about that [11] after you read it, you could write me a letter [12] and we'll try to explain essentially what it [13] boils down to, the discovery ruling and then [14] the setting of a date.

[15] With regard to the pretrial order, [16] I sound like a broken record sometimes at these [17] conferences, but you list witnesses, for [18] instance, on behalf of Power Integrations, you [19] have like seven people that you say are going [20] to testify and then there's a list that is a [21] little more extensive and there's the cryptic [22] statement that these folks may be called in [23] rebuttal, they may come to Wilmington for [24] lunch, I don't know what they're doing in the

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[1] pretrial order, but, you know, you got to [2] pretry the case.

[3] So what has to happen is both sides [4] have to — and it's important for the [5] allocation of time, you have to tell me who the [6] witnesses are going to be and then I can make [7] decisions about whether there's too many, [8] they're accumulative, there's some question [9] about the offer of their testimony. But I need [10] to know exactly who the witnesses are going to [11] be and it would seem not illogical that they [12] would be — that they'd be listed in the order [13] you intend to call them and a little bit about [14] what they're going to say.

[15] There's no surprises in this case, [16] so there's no rebuttal witnesses, other than a [17] planned rebuttal witness to an answer, and I [18] call that more of an answering witness but it's [19] fairly characterized as a rebuttal witness. [20] But we would know who they are and it's just a [21] question of putting it on logically and [22] consistent with the order of proof so the jury [23] gets, well, this is what they said with the [24] burden and this is what they answered and this

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[1] is our rebuttal or answer to that, but that has [2] to be set out.

[3] And then you know exhibits would be [4] — there's a certain volume of exhibits in a [5] patent case that I allow to come in just for [6] the record because you think you might need it [7] later on but they never get shown to the jury [8] and they're part of the pretrial order and [9] admitted in the record. But I really need to [10] know exactly the — and I never put lawyers to [11] this test, but, you know, sometimes you can [12] actually tell us with what witnesses they're [13] coming in and who's testifying about them but [14] maybe that's too difficult. But at least [15] you'll be able to say exactly what exhibits are [16] going to be presented with testimony before the [17] jury and that gives me some idea of how to make [18] decisions again about time, also about any [19] objections that may be offered. Both of those [20] are going to have to be tightened up in this [21] proposed order. And I guess depending on when [22] we pick a trial date I'll give you an amount of [23] time to get that done.

[24] With regard to the case, the

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[1] validity case, the invalidity case, I'm [2] seriously thinking about separating that from [3] infringement and damages. And without knowing [4] something that would be prejudicial or unduly [5] prejudicial, I'm inclined to do that.

[6] **MR. GUY:** If I may be heard on [7] that, Your Honor?

[8] **THE COURT:** Yes.

[9] **MR. SPEAKER:** We have suggested [10] bifurcation — Fairchild has suggested. What [11] we would like to do there is because of some [12] issues that are ongoing right now with respect [13] to damages, we still have a number of [14] depositions to take. The experts have not been [15] deposed, the two damages experts. We need to [16] propound or provide a 30(B)6 deposition on U.S. [17] manufacturing, should be a limited deposition.

[18] Also, there has been an undisclosed [19] expert that — or unnamed expert that is [20] provided, expert reports in end of April, early [21] May, so that would tend to move that issue of [22] damages, all the damages related issues out.

[23] The other point though is that the [24] damages experts, particularly the plaintiff's

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[1] damages experts, relies upon Power Integrations [2] financial statements, their filings, annual [3] reports, and quarterly reports with the SCC.

[4] There is currently an ongoing [5] investigation apparently going on at Power [6] Integrations. They have not filed their 2005 [7] annual reports. They have notified the SCC [8] that all prior reports are unreliable. I want [9] to make that clear that all prior SCC reports, [10] annual reports, quarterly reports going back to [11] 1999 are unreliable. They'll need to be [12] restated. And in addition, Your Honor, they [13] expect to have those — according to the [14] information we have and it's not subject to [15] discovery, but they would have that information [16] to NASDAQ by August the 2nd. I don't know [17] whether they'll meet that or not.

[18] They have been up in front of the [19] NASDAQ board twice on delisting issues [20] regarding their failure to provide these [21] reports. So this is a fundamental issue that's [22] going on. The damages experts have relied upon [23] these. It relates to back dating of stock [24] options. It's our understanding that both the

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[1] chairman and the chief financial officer have [2] been fired related to this issue. We know that [3] they've resigned and left the company at the [4] same time this was going on. So this is a [5] material issue and, again, it all relates to [6] damages and I'd ask the Court to consider that [7] in terms of bifurcation in terms of pushing the [8] damages component off.

[9] Thank you, Your Honor.

[10] **THE COURT:** Thank you.

[11] **MR. SCHERKENBACH:** I didn't hear

[12] any substantiative argument as to why the [13] issues couldn't be divided in the way you [14] suggest. I'm perfectly happy with that. It [15] makes quite a bit of sense to do it. So [16] infringement and damages in one trial, validity [17] in other.

[18] I don't know if Your Honor has in [19] mind the same jury or different juries. I [20] might have some concerns if we're talking about [21] different juries or if there is a substantial [22] subrogation but I suppose we could talk about [23] that.

[24] To respond to Mr. Guy's point, the



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[1] further discovery is minor. The two damages [2] experts need to be deposed. We've been tying [3] to schedule that for some time. That will [4] happen shortly.

[5] The witness Mr. Guy referred to [6] relating to Manufacturing, you may have seen [7] this, Your Honor, in the pretrial papers, but [8] there had been an issue in the case about the [9] extent to which Fairchild manufactured the [10] accused products in the U.S. Fairchild is [11] saying essentially they never did that and [12] Power Integrations is a little skeptical.

[13] It turns out Mr. Kim, the elusive [14] Mr. Kim whose deposition we finally got, you [15] may recall you ordered that. He said, well, [16] actually, in fact, they did manufacture in the [17] U.S. This just came out in the last several [18] weeks. We were surprised because we've been [19] told the contrary. And Fairchild then went [20] back to the drawing board, investigated it and [21] said, yes, it turns out that several million of [22] the accused parts have in fact been [23] manufactured in the U.S.

[24] So we agreed that as a result of



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[1] that we now get at least one further deposition [2] on the extent to which the U.S. manufacturing [3] actually occurred. It's one deposition. There [4] will be some additional, I think, document [5] discovery that's required but it's not the sort [6] of thing that's going to cause any sort of [7] significant delay.

[8] The financial statement point, if I [9] can comment on that. There's some truth [10] certainly what Mr. Guy is saying. On the other [11] hand, with all due respect, in our view is a [12] sideshow. It doesn't have anything to do with [13] the damages information that's relevant to this [14] case.

[15] Yes, there are some SCC statements [16] and filings that are going to be revised. The [17] portions that the SCC filings were relied on by [18] either expert have nothing to do with stock [19] options, date of grants, so forth. That's [20] really just a sideshow and shouldn't derail [21] what the scope is in the case.

[22] **MR. GUY:** Your Honor, first of all [23] with respect to the U.S. manufacturing issue, [24] we were unaware that this was going on and what



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[1] happened in that case is approximately single [2] digit percentage, five percent or so, certain [3] parts, one part in particular was manufactured [4] in the U.S. very, very briefly.

[5] Mr. Kim's testimony was he did not [6] know whether there was U.S. manufacturing or [7] not; however, a document was produced during [8] that deposition and that's what triggered the [9] investigation.

[10] With respect to the issue about the [11] stock option and issues like that, it has to do [12] with what their true expenses are. It has to [13] do with what their true costs in the case are [14] and they're claiming huge loss profits and huge [15] price erosion claims here basically over a [16] rather minor amount of U.S. sales.

[17] Even if you take their numbers, I [18] think they say that 23 percent of our product [19] comes into the United State, and this is about [20] $27 million worth of worldwide, so we're [21] talking about maybe $6 million in the U.S. and [22] yet their damages claim is $45 million to be [23] trebled to total some $135 million.

[24] **THE COURT:** So the damages claim, I



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[1] thought I read, was like 5 or 6 million in lost [2] profits and then there was this price erosion [3] claim in twenties of million.

[4] **MR. GUY:** Yes.

[5] **THE COURT:** How does it get to 45 [6] million? Does that add up to something more?

[7] **MR. GUY:** Yes, if you add it all up [8] it ends up being — the last page under Tab 2 [9] there's 5.9 million lost profits, lost profits, [10] damages and price erosion is 29, almost 30 [11] million, and reasonable royalty is another 6 [12] million.

[13] **THE COURT:** Okay.

[14] **MR. GUY:** So that's about 40 [15] million.

[16] **THE COURT:** I was leaving out the [17] reasonable royalty because that wasn't [18] implicated in your argument about the relevance [19] of the cost factor of whatever is going on with [20] the filings.

[21] **MR. GUY:** I think it does in terms [22] of a hypothetical negotiation about what a [23] reasonable buyer and reasonable seller would [24] come to about what their true profit is. I



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[1] think it would be relevant to that even for [2] reasonable royalty. Assuming that's correct, [3] we still have $36 million in lost profits and [4] price erosion and their financial statements [5] clearly depend upon that. That's what they [6] are. They report their profit a loss.

[7] With all due respect to [8] Mr. Scherkenbach, he can't stand up here and [9] tell you what the restatement will be, how much [10] will the amounts vary. All we know are the two [11] key members of Power Integrations have been [12] fired over this and that they have filed [13] statements with the SCC saying that it's going [14] to be material.

[15] **THE COURT:** You're from a large [16] firm. This is 2006. This is corporate [17] America.

[18] **MR. GUY:** Yes.

[19] **THE COURT:** I don't mean to [20] belittle it, but a couple executives get fired, [21] a few restatements, a few false filings, I [22] mean, you know, I don't even know anymore.

[23] **MR. GUY:** Your Honor, that's [24] exactly right and neither do we and nor does



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[1] Mr. Scherkenbach.

[2] **THE COURT:** I don't know if that's [3] real important stuff anymore. I used to be a [4] prosecutor. I thought I understood what crime [5] was. I really did. I thought I had a handle [6] on it for about 20 years. I'm not sure I [7] understand what crime is anymore. You can rape [8] somebody and go to jail for three years, and [9] I'm not belittling it, but if you steal a few [10] million you get 25 years. I'm not working the [11] numbers well. I'm glad I'm getting out of this [12] profession soon.

[13] **MR. SCHERKENBACH:** Don't say that.

[14] **THE COURT:** I shouldn't be glad I'm [15] getting out?

[16] **MR. SCHERKENBACH:** No, don't say [17] you're getting out of this profession.

[18] **THE COURT:** I'm going to take up [19] boating. Everybody is real nice. They help [20] you.

[21] **MR. SCHERKENBACH:** Judge Maher used [22] to say he was going to take up mullet spotting.

[23] (Brief discussion off the record.)

[24] **THE COURT:** But I understand what



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[1] you're saying and I'm going to five you a [2] chance to get some information, but like, you [3] know, damages are an important issue here and [4] I want you to have as good a handle on what [5] evidence is available.

[6] I'm one that's not going to be too [7] persuaded by a lot of what goes on in corporate [8] governs. I'm interested in damages would be [9] the second route because you can't get to [10] damages unless you have a verdict on [11] infringement, so that's important.

[12] And then if you have a verdict on [13] infringement, it's important to know whether [14] the patents are valid. That's the way I kind [15] of look at things. I don't see any crime going [16] on in infringement invalidity, unless I live [17] another year maybe I will. Because I feel bad [18] for you lawyers and what they're doing with the [19] patent and trademark office.

[20] Anyway, let me say this, I'm going [21] to give you a chance. I think what you're [22] really asking me, Judge, can you hold off. [23] Because I'm not going to try this case in the [24] summer anyway. I have two other patent cases.





[1] You're looking at a fall trial date so we have [2] some time.

[3] But I do want you to tell me — let [4] me tell you my thought about separation of [5] issues rather than bifurcation. I'm willing to [6] separate issues because I have concerns in [7] patent trials, having done a number of them, [8] that there's a lot of overlapping evidence that [9] becomes prejudicial, unduly prejudicial. I've [10] convinced myself, which is pretty easy to do [11] when you talk to yourself, that it's important [12] that if you separate infringement invalidity [13] that they ought to have a different jury. And [14] the first injury ought to hear about [15] infringement and possibly damages.

[16] The second jury ought to hear that [17] the person accusing the patent of being invalid [18] has been found to infringe. That's all they [19] need to know. These defendants were found to [20] infringe and they claim that the patents are [21] invalid, so you're going to get to decide [22] whether the patents are invalid. And, again, [23] in my mind I've reasoned that that's a real [24] fair way to try a patent case.





[1] Now, there's obviously issues on [2] both sides they'd rather have some sort of [3] overlap, maybe and maybe not. But the real [4] issue I focus on is whether or not it violates [5] the Seventh Amendment about jury trials. [6] Federal circuit doesn't seem to have the [7] stomach to take that issue up. But they have [8] said that separation of issues is not a bad [9] thing from when Chief Judge Maher was there [10] he's kind of like when he wrote early on and [11] others have what they've written is that they [12] think it's a good idea.

[13] And so the only issues I can focus [14] on is whether or not a second jury violates [15] lays someone jury trial right. I guess as long [16] as it's still a jury how can it do that? I [17] haven't been able to find a way or heard a good [18] argument that it does.

[19] So let me say this, in your case [20] you got to work on your witness list. You got [21] to work on your exhibit list. So it's really a [22] pretried case. You have to understand you're [23] going to have separation of issues. I'm [24] inclined strongly toward infringement and





[1] damages and then validity. And I'm inclined to [2] two separate juries with some spread of time [3] between the infringement and damages verdict. [4] Of course if it's four defendants then you [5] don't try the validity because you don't go [6] after a patent that you don't infringe. But if [7] there is infringement, then we would have the [8] validity case maybe in a month or so after [9] that.

[10] And, again, let me make this clear, [11] I don't do that so that there's pressure on [12] people to settle. I don't worry about [13] settlement. I just do it because it gives you [14] time to think about your case and get ready and [15] you're not coming right off the trial on the [16] first set of issues. So then we would have [17] that second trial.

[18] Now, I'm willing to listen to [19] anything you want to tell me about — you [20] obviously think that damages ought to be put [21] off even further, as I understand it.

[22] **MR. GUY:** Yes, Your Honor. At [23] least until the numbers are set. I understand [24] your point about crime. I understand the





[1] issue. But the point being here is that all we [2] know is the numbers that both experts have [3] relied upon are unreliable and we need to know [4] what those numbers are. And hopefully we'll [5] have it by August, but at the same time —

[6] **THE COURT:** You said August 2. [7] We're thinking about a fall trial.

[8] **MR. GUY:** We need to talk about a [9] trial date, if you're talking October, [10] November, I think it would be plenty of time [11] but I understand there may be conflicts.

[12] **MR. SCHERKENBACH:** Your Honor, on [13] this financial point, you've indicated that [14] you're inclined to give them some further [15] discovery. I guess we can live with that. I'm [16] frankly disappointed in it because what they [17] want to do is have a fifth day of depositions [18] with my CEO who they've had for four days.

[19] You may remember there was a [20] dispute over the fourth day. But it's a [21] sideshow. If we have to do that to stay on [22] track here we're willing to do it.

[23] **THE COURT:** I'm inclined, based on [24] what I'm being told today, if the supplemental





[1] filings or substitute filings are about matters [2] that are different than are being argued here [3] today and you can demonstrate they're just [4] nothing relevant to what's going on in this [5] trial I may not be inclined.

[6] **MR. SCHERKENBACH:** I appreciate [7] that clarification. I think we at least will [8] be able to make that showing and we'd like an [9] opportunity to do it. It's stock option [10] related. It's non-operating expense. It has [11] nothing to do with the operating profit. It [12] doesn't affect the revenues. It doesn't affect [13] the cost of manufacturing or other costs.

[14] So the thing that the patent [15] damages experts rely on are not going to change [16] a bit as a result of this and we'll be able to [17] show that to you.

[18] In terms of separating the issues, [19] just to respond to your proposal, infringement [20] and damages in one trial to one jury, validity [21] to a later jury. I'll be able to accept that [22] on behalf of Power Integrations. I'm not going [23] to make a Seventh Amendment argument. I [24] understand one probably could be made, but





[1] we're not going to get an answer to that anyway [2] in time to matter.

[3] I think as long as the second jury [4] though is told that what the outcome — without [5] embellishment of what the outcome in the first [6] case was, I think that's important.

[7] **THE COURT:** When I've done it I [8] have the jury understand that there has been an [9] infringement finding but nothing else. We [10] don't talk about the damages award if there is [11] one. We just say there's been an infringement [12] finding but under the law now there's a [13] challenge to the validity of the patent

that's been found to infringe. It puts it real nicely before the jury. They understand that. But it gives you eight new people who hear the validity fresh so there's not any prejudice to the presentation of either sides validity case.

**MR. SCHERKENBACH:** And, again, I can accept that on behalf of my client. I've been through that before with Judge Robinson. I thought it worked reasonably well. Despite what defendants tend to think, it tends to be pretty fair.





My major concern is drawing it out. You mentioned fall, that's great. I'm very much hoping we can get September for the first trial, some time in September, and a delay of maybe no longer then until December or so for the second one. We don't want to drag it out.

**THE COURT:** I was thinking I can sort of give you a range.

**MR. SCHERKENBACH:** That would be great.

**THE COURT:** And I want to give you some dates to revise, what I need revised and presented. Let me go to my manually electronic calendar here.

September has been eaten up by Lucent versus Extreme. They're back for a retrial. I have to hear them. That's a retrial. I granted a motion for a new trial and we set that date a long time ago, so there's really difficulty in getting in September.

However, October, the early part of October is available.

**MR. GUY:** That's fine with us, Your





Honor.

**MR. SCHERKENBACH:** My wife is going to kill me. We're expecting our third on the 8th. I was hoping I could avoid a direct train wreck.

I, also, I'm in trial with Judge Robinson the beginning 30th of October for three weeks, so if we could work around that, maybe start a little after the eight and continue it in that way. I don't actually have the days of the week. Actually, here I do. Okay.

**THE COURT:** I'll tell you what's going on in October. The week of October 2nd — and I don't want you here if your wife is giving birth to your third child on October 8th, so they're the two blank weeks I have in October. Starting the week of October 16th Affymetrix wants to sue Illumina, and Sun Power Company from Puerto Rico wants to sue another power company and they're double scheduled to share the trial day.

And then the week of the 23rd of October, a company called Trilogen wants to





sues Martese for patent infringement and they'd like to be here for seven days.

So other than those first two weeks that sort of eats up October. But we could go to the week — the first week of November, which is actually — it's available and then we could go thirty days later in December.

Now, remember, when there's separation of issues you don't need as much trial time as you needed if you have everything together, obviously. You could go the week of December 4th. So you could have the week of November 6th and then the week of December 4th. It my run in to the following week on either scheduling but that would be fine.

So if those dates work, that would give you enough time to have the August 2nd filing and some discovery if it's ordered and —

**MR. GUY:** Your Honor, my understanding then we'd only have one week to do damages and infringement?

**THE COURT:** Well, maybe only three days.





No, I didn't want you to grab your chest.

**MR. GUY:** I do workout. It's not too dangerous to hear things like that.

**THE COURT:** Typically here infringement, validity and damages you get ten trial days. That's why we're able to try as many cases we do. If we gave everybody what they wanted, we'd never do what we do.

Actually, the week of November 6th. What I was saying is I have the ability to go in to the next week if you eat up more than let's say five or six days. We can do that on the infringement, damages. And, again, on the December date I can go in to next week. But I can't allocate time until I actually see a good pretrial order and a number of witness and I can measure how much time I'm going to give each witness based on what they're going to say.

So the answer is don't be nervous about that. I'm only saying that's the week we'll start. There's enough time to get seven days if we need it.





**MR. SCHERKENBACH:** I have a markman hearing that's already scheduled on November 15th.

**THE COURT:** You'll be out of here by November 15th, I'll guarantee it, unless the jury is deliberating. There's no way you would be here on infringement and damages November 15th.

**MR. GUY:** We need to raise one other issue, Your Honor, and that has to do with some jury insufficiency in the pretrial order, Power Integrations disclosure. There are 38 products that are accused of infringing 18 claims. And just to March through that, Your Honor, I think — and just 18 claims, Your Honor, in three days is huge.

**THE COURT:** Mr. Scherkenbach has been here before. He knows we're not going to have 38 products.

**MR. GUY:** Well, there are four groups of product, Your Honor, that statements at face value isn't very helpful. We will pair down the number of claims further.

**THE COURT:** The claims are going to





be paired down.

**MR. GUY:** The claims will be paired down. The products we'll break down in to only three or four groups. 38 is not a real meaningful number. I'm not prepared to say we'll drop whole groups of products. I think the case can easily be tried in groups, in fact, the experts on both sides have dealt with them in that way, so it's not a real —

**THE COURT:** Four categories of products are different than 38 products. 18 claims is 18 claims. That has to be cut back which you're acknowledging.

**MR. GUY:** Absolutely. We have four patents so it works out one per — I think one of them you only have two claims that's asserted. If we're pairing it back to one claim per patent, that would certainly make it doable. But still these technologies are different. Even though three of them are circuit patents, they do different things. So it is important we recognize that what we're asking the jury to do is to consider at least 16 different permutations of four product





groups versus at least four patent

claims and four different patent. So I'm anxious to see how it's going to be paired down and I think we can have a meaningful understanding in a more thorough pretrial conference state once we know that.

**THE COURT:** You know, there's no order prohibiting both of you from talking about that.

**MR. GUY:** We have asked, Your Honor.

**THE COURT:** Well, it's, you know, actually having a discussion about what might be reasonable and then if you have dispute bring it to me. But here's what I'm — I'm not discussing that today because I recognize that there's some ugliness in other parts of pretrial order, but usually what sets the tone is who's going to be the witness and what they're going to testify about and what exhibits you're going to use.

When I get done addressing those two categories of the pretrial order, I think a little more will become apparent, a little more





of what you have to do will become apparent. If you haven't gotten it done by addressing witnesses and the exhibits.

And when you address witness exhibits they should be addressed in the present understanding of infringement, damages and invalidity. And that should go a long way in pairing down. And you should have discussion with each other, and then if you can't agree then I may have to weigh in.

**MR. SCHERKENBACH:** Can I go back to scheduling for a moment?

**THE COURT:** Yes, you can.

**MR. SCHERKENBACH:** People seem to get a little bit interest in November. That is when I'm in trial if front of Judge Robinson, so October 30 to November 24th. I think that case is highly likely to go. What I would request is that we take the first week of October.

**THE COURT:** You're in a four week trial?

**MR. SCHERKENBACH:** It's two defendants, multiple patents. I think that





will be paired back to probably two weeks at the end of the day. Judge Robinson did bifurcate damages. Nonetheless, the first two weeks in November won't work for me. I'd be happy to take the first week of October because I don't believe damages and infringement will take more than five trial days by anyone's stretch of the imagination and then we can perhaps take the first week in December for validity trial if necessary. That would work.

**MR. GUY:** That's fine with me, Your Honor, as long as we have the ability to overflow into the second week of October if need be.

**MR. SCHERKENBACH:** I think that's fine. Once Your Honor sees the revised pretrial you can make that decision as to whether it requires that much trial time. I don't believe it will.

**THE COURT:** All right. October 2nd, for present purposes, will be the commencement of — Monday, October 2nd will be the commencement of infringement and damages, and December the 4th will be the commencement





of invalidity.

And both sides understand that there will be time allocations set, which I don't know what they'll be yet because I don't know what the witness list looks like or the exhibit list.

**MR. GUY:** We also have an issue of inequitable conduct in this case. That will be tried during the invalidity section?

**THE COURT:** I don't send that, for any purpose, to the jury. I'll listen to the evidence and then I'll issue a decision post trial.

And if you need to present a witness outside of what's presented to the jury, I'll spend the time to hear that one or two witnesses after the jury section is over some day or at a day after the jury evidence is complete.

**MR. SCHERKENBACH:** Very good.

**THE COURT:** Here's what I'm going to do, I'm going to set a second pretrial conference and a date to submit a revised pretrial order along the lines that I've





indicated here.

The second pretrial order will be due Friday, September 1, and then the second pretrial conference — what are your schedules looking like in September? Do you want to come a couple weeks before the trial?

**MR. SCHERKENBACH:** Yes, Your Honor. Fine for Power Integrations really any time in September.

**MR. GUY:** I have a conflict on the 11th, that's it.

**THE COURT:** Okay. So let's see, the 11th — I guess traveling is better in the middle of the week, right, then getting near the end. So do you want to come for the second pretrial conference on either the 13th or the 14th of September?

**MR. GUY:** 14th would be better, Your Honor.

**MR. SCHERKENBACH:** That's fine with me, Your Honor.

**THE COURT:** All right. We'll do it on the 14th of September, which is a Thursday, and we'll do it at I guess 1:30. Does that





work?

**MR. SCHERKENBACH:** Yes, Your Honor.

**MR. GUY:** Your Honor, we have an issue of motions in liminae in the case. Can we take up the hearing on the motion in liminae or briefing schedule for the September 1st date?

**THE COURT:** Yes, you can agree to that. What I typically will do is at the pretrial conference that actually is anticipation of a set trial I will give you my rulings at that pretrial conference. So you should give me enough time to read whatever it is you're going to write before that pretrial conference. So if it's the 14th, you probably should get it here that Monday or the Friday before and then we'll take a look at it and give you the rulings on the pretrial conference.

**MR. GUY:** So, in other words, you would like to have briefing completed by September the 4th, that would be the Monday the week before?

**THE COURT:** No, just the Monday —





**MR. GUY:** The 11th?

**THE COURT:** That would be fine if you got it here by then. You know, it's granted or denied. It doesn't take a lot of effort if you get excellent briefing. The decision is as good as what the argument is, right?

**MR. GUY:** Absolutely.

**THE COURT:** Unless minimally skewed.

**MR. SCHERKENBACH:** Can I ask Your Honor how you're handling the issue of experts beyond the scope of report? Is it the same way you have been in the past?

**THE COURT:** Absolutely.

[16] **MR. SCHERKENBACH:** I think that [17] will help resolve a number of things.

[18] **THE COURT:** Right. That's one of [19] my, what is it, we all get 27 great ideas and [20] I'm working on 4,011. That was one of the [21] great ideas. It really works. I've now [22] ordered new trial. It's not good if you play [23] around with the expert report.

[24] You know that practice.

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[1] **MR. GUY:** Perhaps I should hear it [2] clearer from you, Your Honor.

[3] **THE COURT:** I'll give it to you [4] straight up here. Everybody argues over expert [5] reports and then the expert gets to trial and [6] of course there's something alleged to be [7] different, some new opinion, some nuance on an [8] opinion, particularly after the other side has [9] taken advantage of the opportunity for [10] deposition under the rule.

[11] My practice is in a trial, a [12] serious trial with a jury, or even in a bench, [13] I guess, but particularly the jury, I don't [14] have time to go back and read the report and [15] make an evidentiary ruling on the expert's [16] testimony, so you have to interpose your [17] objection.

[18] If you think the witness is [19] testifying outside of the report and deposition [20] or if it's just a report of the report, if post [21] trial you maintain that objection and I take a [22] look at it and in fact there is some variance, [23] and I mean "some," it doesn't have to be a lot, [24] something that I think could have affected the

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[1] other side to their detriment because it wasn't [2] disclosed, I simply say that there's a mistrial [3] and the other side pays the cost of the first [4] trial and we go to a second trial.

[5] It puts a lot of burden on the [6] attorneys but it's, you know, how can you have [7] experts — I mean discovery. I used to find [8] after trial that in fact the witness deviated [9] substantially and what do you do then? You [10] know, you're kind of interested in keeping the [11] verdict and things like that but it really [12] isn't fair during a trial in my experience, so [13] that's the practice.

[14] **MR. GUY:** Your Honor, both sides [15] filed supplemental expert reports in light of [16] other fact discovery that was ongoing and we [17] still have an issue, certainly if there's a [18] debate 30 days before the trial in which the [19] expert reports are filed by that point, any [20] variance from that is certainly understandable. [21] You're not addressing issues where there's been [22] an ongoing fact discovery and expert report [23] comes in to supplement?

[24] **THE COURT:** No. You all, as I

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[1] understand it, have a little more your want to [2] do. So get it done, pick a date, if you can't [3] pick a date I'll give you one. It will be some [4] time in August.

[5] **MR. SCHERKENBACH:** For damages I [6] think that's fine. This doesn't bear on [7] liability at all?

[8] **THE COURT:** No, liability from what [9] I saw in the proposed pretrial order is clear. [10] So you will get that date. And what you're not [11] allowed to do is to send a letter like a week [12] before trial saying the witness just told me [13] this and I'm going to add this or something. [14] So whatever that date is, that's what you're [15] locked in to as a report and deposition.

[16] **MR. GUY:** Your Honor, just so we're [17] clear, we had an expert who did add additional [18] prior art at a deposition. As long as that's [19] in a report by this cutoff date, that should be [20] okay. We'll certainly make sure that whatever [21] he testified to is actually contained in that [22] report.

[23] **THE COURT:** That's pushing the [24] envelope a little bit because damages, by your

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[1] request, has opened up a little bit.

[2] **MR. GUY:** Yes, Your Honor.

[3] **THE COURT:** We have expert dates [4] and I know we all get up every day and have a [5] better idea than we had yesterday, but in [6] litigation we really have to tell the expert [7] that there's a date where you can't think [8] anymore. And I'm trying to say this very [9] simply.

[10] So if a new piece of prior art came [11] in but there's been a cutoff date, they're [12] stuck with that cutoff date. We have to limit [13] the discovery and the opinion offering.

[14] Now, if in this case, because the [15] trial date is some time off, you can both agree [16] that you want to — but I wouldn't let that be [17] an August date on liability. That's too close [18] to the trial date. But if by July or something [19] you want to extent it and you want to [20] supplement reports, get them all cleaned up, [21] but you got to on expert opinion testimony [22] there has to be a date when it ends.

[23] In a medical malpractice case and [24] the guy comes in, the doctor, a surgeon, wants

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[1] to talk about an operation he had last week, [2] how are you supposed to prepare for that? At [3] some point — because he learned something. I [4] believe he did. Then they say you can [5] foreclose. You have to foreclose.

[6] **Mr. GUY:** Your Honor, we can [7] certainly set a date this summer in which [8] everything will be final and we have the other [9] discovery to do. I just want to make sure that [10] to the extent the expert has provided testimony [11] on something, that we can make sure it's in, [12] we'll go back and make sure if any supplement [13] report is due we can probably do it by the end [14] of June, first of July and give them plenty of [15] time.

[16] **THE COURT:** Do you have a problem [17] with that?

[18] **MR. SCHERKENBACH:** We do because [19] the deposition has happened. It's done and [20] over with. This is actually one of the motions [21] in liminae. Not that I expect the Court to [22] even look at them at this point, but there's a [23] particular person they have in mind who [24] substantially changed his opinions at

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[1] deposition and without supplementing the report [2] and we were told, well, you've had a chance to [3] ask questions, ask him questions at deposition, [4] that's too bad.

[5] So what I'm sure they'd now love to [6] do is have a date in the future that they can [7] put it in a report. I guess we'll depose him [8] again. We object to that. That's over. It's [9] a very limited window to do damages expert [10] reports — discovery, excuse me, reports are [11] done. Finish those, a will bit of clean up and [12] that should be that.

[13] Maybe this is something Your Honor [14] decides in motion in liminae and if we lose we [15] have to go back to the drawing board. We're [16] doing a mock trial next weekend. I need to [17] know what the case looks like, what it's going [18] to be. I think I do on the liability side and [19] we're preparing for trial. I should not have [20] to be redoing liability expert discovery.

[21] **THE COURT:** I'll tell you what that [22] motion in liminae gets you a decision, then [23] you'll know whether you can — see, one of the [24] things, if what I'm hearing is factual, if the

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[1] witness changed at the deposition what the [2] opinions of the report were,

that's an egregious violation of the scheduling order because how would you ever prepare for a deposition except from the report, and then when you showed up if there were new opinions that weren't in the report, what would be the sense of a deposition?

**MR. GUY:** Your Honor, he did not change his view in the report originally. What he did was he supplemented with additional prior art and also with an obviousness argument that he provided them with a clear shot at it at the deposition.

**THE COURT:** That's my point. Let's assume he added a piece of prior art and modified his opinion. It's like the surgeon that comes in and says last week I had a cardiac operation, let me tell you what I did. So I go to the deposition, you know, I'm prepared and done and happy, and all of a sudden he starts talking about prior art because it's not in his report, how did I prepare for that? So how did I intelligently





conduct the deposition, which is my opportunity to get further information about the opinions in the report?

**MR. GUY:** They were certainly aware on notice that there was obviousness issue. There was certainly notice on prior art. They certainly had an opportunity and all we wish to do is preserve what is already in a deposition for trial.

**THE COURT:** I'm asking you, we're just having a conversation here, we're not a accusing anybody.

**MR. GUY:** Furthermore —

**THE COURT:** How would I have prepared for that deposition if I didn't know about the new piece of prior art?

**MR. GUY:** You would have gone in and you would have prepared for obviousness. You would have learned about the additional prior art. You would have asked questions related to obviousness.

**THE COURT:** I would have done that?

**MR. GUY:** Furthermore, I forgot this, but it was in part in response to their





rebuttal report. So it's a lot more involved in this than just we surprised them. They certainly had an opportunity to cross the expert. They had an opportunity to go in. If they needed more time, they had that, also. So all we're trying to do is preserve what's in a deposition. It was right after the markman hearing, so it would have been late February or March. So they had ample opportunity. There's no surprise like on a witness stand when someone talks about what they did last week. We have all summer, Your Honor, to address this if there's an issue. We just want to be able to get the evidence in for a validity issue which isn't going to trial until December, so there's ample opportunity here to address this rather than trying to strike some evidence that they feel that they don't like.

I would also add that at least in one instance that where we were aware of the art through one of their experts, so, you know, it does take a little bit of iteration here to get all the evidence in and all the expert





reports right. We certainly will not deviate from the expert reports once they're final. And we can make that final date July.

**THE COURT:** See, there could be a book written, or at least a chapter, that you and I could do in a patent trial treatise. Because my view would be, and I'm not an advocate, is that the deposition is the trial date in the context of the scheduling order for expert discovery. That's the drop dead examination day.

But you have the view of 95 percent of the lawyers that come here, which is understandable because you need some iteration, you need to play a little bit, you got to find out, then they put a rebuttal and I have to respond to that.

But that, in my view, runs completely against all of the rules of procedure. So why did I do a scheduling order and have expert discovery dates? They're like the world ends on those dates. There is no other day. And they're drop dead dates.

So when that witness comes in and





has a new piece of prior art, which is the practice, I mean, that's what the lawyers do, then you open up the date.

**MR. GUY:** I understand but I think it's one of degree. We're not talking about we submitted two pieces of prior art.

**THE COURT:** You're getting nervous. Don't get nervous I'm going to foreclose. You're getting nervous. We're just having a conversation about the real world versus Civil Procedure 1 in law school. There's actually people that think that there are dates that count.

I might let you have this in. I have to see what was said. But how do we get lawyers to understand that they are drop dead dates and there is no iteration beyond that date? I mean, the world ended for purposes of that discovery. And it doesn't matter whether they learned which was until then truly not able to be found by them some new information, how do we package a trial if we keep having 95 percent of the lawyers think that the dates have some sort of elasticity in them, you know,





they can be just pushed a little bit? It's really hard. But we're not going to solve that today.

What's the motion in liminae I got to look at?

**MR. SCHERKENBACH:** No. 2, Your Honor, on Power Integrations list. This is tab 16 the second item.

**THE COURT:** We'll get you a quick answer from Tab 16 on No. 2.

**MR. SCHERKENBACH:** I assume you'd like us to — do you want short letter briefs on this or —

**THE COURT:** Sure. Because the motions are only listed.

**MR. SCHERKENBACH:** Yes, just identifies the issues. So we can get you a short letter brief in say a week.

**THE COURT:** That's fine. And then we'll get you the answer.

**MR. GUY:** Your Honor, would we be also allowed to — they've done much the same and we would like to file a similar motion in liminae on the same issue if they're going to





do it this way.

**THE COURT:** In the legal profession it's always fair to punch back.

**MR. GUY:** Just wanted to make sure.

**THE COURT:** Sure.

**MR. SCHERKENBACH:** Which one is that, Mr. Guy?

**THE COURT:** How would we maintain the adversary system if we didn't punch back? It would just collapse. We'd have lawyers with low blood pressure or something.

Which one do you want to punch back with?

**MR. GUY:** Under our Tab 17.

**THE COURT:** This is the limit now.

This is dropping dead. I'm not going to look at any others.

**MR. GUY:** In terms of?

**THE COURT:** In terms of opening up any kind of expert discovery beyond the damages that you've argued you can't get done because of the August 2 filings, anticipate filing.

**MR. GUY:** In our motions in limine —





**MR. SCHERKENBACH:** And I don't believe Your Honor to raise one that relates to this issue.

**THE COURT:** Let them look at my filing. Give them a chance.

**MR. GUY:** The first one is defense motion in liminae, motion to exclude untimely reports in an undisclosed expert.

**THE COURT:** They got you pretty good there, Scherk.

**MR. SCHERKENBACH:** The expert. If that's the one you want, that's great. No. 1, fine.

**MR. GUY:** Motion with respect to their expert, Troxel, I believe all of those deal with there is an untimely report there as well. I think it's item No. 3 under 2.

**THE COURT:** No. 1, 2. Item No. 3.

**MR. SCHERKENBACH:** I don't think we're talking about damages related stuff. This is liability.

**THE COURT:** If you throw damages in there, you get a yellow flag for piling on.

**MR. GUY:** That was the damage





expert, Your Honor, so we're going to preserve those.

**THE COURT:** We've already said that's a different category. We're going to wait until after August 2 to let you have at each other on damages. This is only liability, that be the context of infringement, validity, expert reports.

All right, your time up. It's a game clock. So you have No. 1, Tab 17 and there's No. 2, Tab 16, and we'll get letters and you'll agree to that schedule for about a week to get them in here and we'll give you expeditious decision so you know where you are.

**MR. SCHERKENBACH:** Thank you, Your Honor.

**THE COURT:** Okay. I think that's all we can do today. I will expect that the one date I got to give you is let's just make it —

**MR. GUY:** I'm sorry, Your Honor, the first letter brief would be due June 7th; is that right?

**THE COURT:** I'm not getting in to





that. You're going to talk with each other and come up with an exchange schedule.

**MR. SCHERKENBACH:** The date for damages wrap up?

**THE COURT:** We need a date for that. It has to be in August because we'll need a couple weeks before the pretrial for any disputes.

**MR. SCHERKENBACH:** The 4th is a Friday. Does that work?

**MR. GUY:** The quarterly reports don't come out until the 2nd.

**MR. SCHERKENBACH:** Okay, the 11th.

**MR. GUY:** You're going to be able to give us a deposition on any changes in that time? Maybe we should push it to the 18th, Your Honor.

**THE COURT:** That would put it beyond the —

**MR. GUY:** It's August the 18th.

**THE COURT:** Oh, August 18th. August 18th is fine with me.

So August 18th is the damages cutoff.





**MR. SCHERKENBACH:** That would be fine, Your Honor.

**MR. GUY:** Be fine, Your Honor.

**THE COURT:** Okay. We'll put this all in an order and get it entered and then look to see those motions in liminae letters.

**MR. SCHERKENBACH:** Thank you, Your Honor.

**THE COURT:** Thank you. We'll be in recess.

(Court adjourned at 1:32 p.m.)





State of Delaware )
New Castle County )

CERTIFICATE OF REPORTER

I, Stacy L. Vickers, Registered Professional Reporter and Notary Public, do hereby certify that the foregoing record is a true and accurate transcript of my stenographic notes taken on May 31, 2006, in the above-captioned matter.

IN WITNESS WHEREOF, I have hereunto set my hand and seal this 14th day of June, 2006, at Wilmington.

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Lawyer's Notes

## D



## E



## F



## G

## T



## U



## V



## W



## Y

Lawyer's Notes

05-15-2005 16:04

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Wilmington, DE

**Press Release** Source: Fairchild Semiconductor

# Fairchild Semiconductor Files Patent Infringement Lawsuit Against Power Integrations, Inc.

Tuesday April 11, 12:36 pm ET

SOUTH PORTLAND, Maine--(BUSINESS WIRE)--April 11, 2006--Fairchild Semiconductor (NYSE: FCS - News) announced today that it has filed a patent infringement lawsuit against Power Integrations, Inc. in the United States District Court for the Eastern District of Texas.



The lawsuit asserts infringement of U.S. Patent No. 5,264,719 by Power Integrations' pulse width modulation (PWM) products. Fairchild intends to take all possible steps to seek a court order to stop Power Integrations from making, using, selling, offering for sale or importing the infringing products into the United States and to obtain monetary damages for Power Integrations' infringing activities.

Fairchild and Power Integrations have been in litigation since 2004 in the United States District Court for the District of Delaware. This lawsuit is a separate action filed in the United States District Court for the Eastern District of Texas.

"What Power Integrations has not been able to achieve in the marketplace, they have sought to achieve in the court room. We are forced to respond in kind. However, in our case, Fairchild is asserting a patent that pre-dates Power Integrations' patents by at least fifteen months," said Tom Beaver, Fairchild's executive vice president for Worldwide Sales and Marketing. "We believe Power Integrations' products are infringing the '719 patent. We will take all possible steps to bring Power Integrations' infringement to a stop and to be made whole for the damages they are inflicting."

Intersil Corporation owns U.S. Patent No. 5,264,719, for High Voltage Lateral Semiconductor Devices, and is a co-plaintiff with Fairchild in the lawsuit. Fairchild has held license rights under the patent since 2001 and more recently secured exclusive rights to assert the patent against Power Integrations.

About Fairchild Semiconductor:

Fairchild Semiconductor (NYSE: FCS - News) is the leading global supplier of high-performance power products critical to today's leading electronic applications in the computing, communications, consumer, industrial and automotive segments. As The Power Franchise®, Fairchild offers the industry's broadest portfolio of components that optimize system power. Fairchild's 9,000 employees design, manufacture and market power, analog & mixed signal, interface, logic, and optoelectronics products. Please contact us on the web at www.fairchildsemi.com.

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**Exhibit B**

To Fairchild's Supplemental Response to Power Integrations' First Set of Interrogatories
June 30, 2005

| '075 Patent | U.S. Patent 5,264,719 |
|---|---|
| 1. A high voltage MOS transistor comprising: | U.S. Patent 5,264,719 ("'719 Patent") describes and claims "A high voltage MOS transistor comprising:". '719 Patent, Claim 8.<br><br>The '719 Patent describes a high voltage MOS transistor. "The present invention provides an improved lateral drift region for both bipolar and MOS devices where improved breakdown voltage and low ON resistance are desired." '719 Patent, Abstract.<br><br>"The present invention relates to lateral semiconductor devices and an improved method of making lateral semiconductor devices. More specifically, the invention relates to high voltage lateral devices with reduced ON resistance and a method of making such devices." '719 Patent, 1:12-16; *see* Figure 10 ("Figure 10 is a cross section of an MOS device, including the lateral drift region and top gate of the invention, in a preferred embodiment." '719 Patent, 3:18-20). |
| a semiconductor substrate of a first conductivity type having a surface | The '719 Patent describes and claims "a semiconductor substrate of a first conductivity type having a surface,". '719 Patent, Claim 8.<br><br>An N-type semiconductor substrate (11) with a surface is shown in Figure 10. "Around the entire periphery of the drift region there is a curved portion $17_e$ which rounds up to the surface of the $N^-$ substrate 11 to insure that the JFET channel in the drift region 17 contacts the MOS channel $11_b$ under the MOS gate 16." '719 Patent, 6:52-56. |
| a pair of laterally spaced pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface, | The '719 Patent describes and claims "a pair of laterally spaced source and drain pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,". '719 Patent, Claim 8.<br><br>P-type source and drain regions (14 and 12) (a pair of laterally spaced pockets of semiconductor material of second conductivity type) within substrate (11) and adjoining the substrate surface are shown in Figure 10. "For the MOS device, the drain 12 is surrounded by the $P^-$ drift region 17 and N type top gate 21." '719 Patent, 6:50-52. "The $P^+$ source 14 and |

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| '075 Patent | U.S. Patent 5,264,719 |
|---|---|
| | $N^+$ body contact $11_c$ are shown as is the dielectric 13 which serves as the gate oxide $13_g$ beneath the MOS gate 16." '719 Patent, 6:59-61 |
| a source contact connected to one pocket, | A source contact is necessarily connected to the source pocket (14) in order for the MOS device to operate. |
| a drain contact connected to the other pocket, | A drain contact is connected to the other pocket (drain pocket 12) in order for the MOS device to operate. "The two contacts, drain contact $12_a$ and body contact $11_c$ are shown for completeness." '719 Patent, 1:27-29. "FIG. 4 shows an MOS device where $P^+$ drain contact $12_a$ is formed in $P^-$ type drain 12...." '719 Patent, 3:37-38. |
| an extended drain region of the second conductivity type extending laterally each way from the drain contact pocket to surface-adjoining positions, | The '719 Patent describes and claims "an extended drain region of the second conductivity type extending laterally each way from said drain pocket to surface-adjoining positions,". '719 Patent, Claim 8.<br><br>An extended drain region (17) of second conductivity type (P) extending laterally each way from drain contact pocket (12) to surface-adjoining positions is shown in Figure 10. "For the MOS device, the drain 12 is surrounded by the $P^-$ drift region 17 and N type top gate 21. Around the entire periphery of the drift region there is a curved portion $17_e$ which rounds up to the surface of the $N^-$ substrate 11 to insure that the JFET channel in the drift region 17 contacts the MOS channel $11_b$ under the MOS gate 16. The drift region 17 extends outward from the entire perimeter of the drain 12." '719 Patent, 6:50-57. |
| a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjoining positions, | The '719 Patent describes and claims "a surface adjoining, top layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain pocket and the surface-adjoining positions,". '719 Patent, Claim 8.<br><br>A surface adjoining top gate (21) of first conductivity type (N) on top of an intermediate portion of the extended drain region (17) between the drain contact pocket (12) and the surface adjoining positions is shown in Figure |

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| '075 Patent | U.S. Patent 5,264,719 |
|---|---|
| | 10. "For the MOS device, the $P^+$ drain 12 is surrounded by the $P^-$ drift region 17 and N type top gate 21." '719 Patent, 6:50-52. |
| said top layer of material and said substrate being subject to application of a reverse-bias voltage, | The '719 Patent describes and claims "said top layer of material and said substrate being subject to application of a reverse-bias voltage,". '719 Patent, Claim 8.<br><br>Top gate (21) (said top layer of material) and substrate (11) are subjected to application of a reverse-bias voltage. "This top gate allows the total channel doping to be increased because the top gate to channel depletion layer holds some additional channel charge when reverse biased in addition to that held by the bottom gate to channel depletion layer of the prior art structure." '719 Patent, 2:44-49. |
| an insulating layer on the surface of the substrate and covering at least that portion between the source contact pocket and the nearest surface-adjoining position of the extended drain region, and | The '719 Patent describes and claims "an insulating layer on the surface of the substrate and covering at least that portion between the source pocket and the nearest surface-adjoining position of the extended drain region, and". '719 Patent, Claim 8.<br><br>A insulating dielectric layer (13) on the surface of substrate (11) and covering the portion between source contact pocket (14) and the nearest surface-adjoining position of extended drain region (17) is shown in Figure 10. "The $P^+$ source 14 and $N^+$ body contact $11_c$ are shown as is the dielectric 13 which serves as the gate oxide $13_g$ beneath the MOS gate 16." '719 Patent, 6:59-61. |
| a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the source contact pocket and the nearest surface-adjoining position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel. | The '719 Patent describes and claims "a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the source pocket and the nearest surface-adjoining position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.". '719 Patent, Claim 8.<br><br>A gate electrode (16) on the insulating layer (13) and electrically isolated from the substrate (11) is shown in Figure 10. The gate electrode (16) controls by field-effect the flow of current through channel ($11_b$) between source contact pocket (14) and the nearest surface-adjoining |

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| '075 Patent | U.S. Patent 5,264,719 |
|---|---|
| | position of the extended drain region (17). "Around the entire periphery of the drift region there is a curved portion $17_e$ which rounds up to the surface of the $N^-$ substrate 11 to insure that the JFET channel in the drift region 17 contacts the MOS channel $11_b$ under the MOS gate 16." '719 Patent, 6:52-56. |
| 5. The high voltage MOS transistor of claim 1 combined on the same chip with a low voltage CMOS implemented device. | It is inherent or would have been obvious to combine the MOS transistor described by the '719 Patent on the same chip with a low voltage CMOS implemented device. |

118/28508CO

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: James D. Beasom

SERIAL NO.: Rule 60 Continuation Application of USSN: 242,405, Filed: September 8, 1988

FOR: HIGH VOLTAGE LATERAL SEMICONDUCTOR DEVICE

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Honorable Commissioner of
Patents and Trademarks
Washington, D.C. 20231

May 24, 1991

PRELIMINARY AMENDMENT

Sir:

Preliminary to the examination of the above-identified application, the following Amendments and Remarks are respectfully submitted.

IN THE SPECIFICATION:

Page 2, eighth line from the bottom, change "drain body" to --drain-to-body--;

Page 3, line 4, change "channel body" to --channel-to-body--;

Page 3, fourth line from the bottom, change "12" to --contact 12A--;

Page 4, first full paragraph, fifth line, change "body drain" to --body-to-drain--;

Page 9, tenth line from the bottom, change "drain body" to --drain-to-body--;

Page 9, fourth line from the bottom, change "gate to drift" to --gate-to-drift--; after "junction", insert --17A--; after "gate" (last occurrence), insert --21--;

Page 10, top paragraph, line 2, after "channel", insert --17--;

Page 10, line 5, change "body to drain" to --body-to-drain--;

Page 10, line 6, change "gate to channel" to --gate-to-channel--;

Page 10, line 7, change "additon" to --addition--;

Page 10, line 13, after "region", insert --17--;

Page 10, bottom paragraph, line 3, change "body to drain" to --body-to-drain--;

Page 10, bottom paragraph, line 4, change "gate to drain" to --gate-to-drain--;

Page 10, bottom paragraph, line 5, after "11", insert --(as shown in Figures 6A, 6B to be described below)--; change "gate to drain" to --gate-to-drain--;

Page 11, line 1, change "body to drain" to --body-to-drain--;

Page 11, line 2, change "gate to drain" to --gate-to-drain--;

Page 11, second paragraph, line 3, after "region", insert --17--;

Page 11, second paragraph, line 6, after "and", insert --N--;

Page 11, second paragraph, line 8, change "effected" to --affected--;

Page 12, line 1, after "and", insert --,--;

Page 12, line 2, after ")", insert --,--;

Page 12, line 9, change "ion implanted" to --ion-implanted--;

Page 12, second paragraph, line 3, after "channel" (first occurrence), insert --17--;

Page 13, line 1, after "region", insert --17--; after "gate", insert --21--";

Page 13, line 2, after "oxide", insert --53--;

Page 13, line 13, after "gate" (last occurrence), insert --21--;

Page 14, line 7, after "17", insert --,--;

Page 14, second paragraph, line 8, change "so" to --as--;

Page 14, second paragraph, line 11, after "11", insert --, via contact region 11C--;

Page 15, first full paragraph, line 4, before "top", insert --N type--;

Page 15, line 8, change "gate to drift" to --gate-to-drift--;

Page 15, line 9, after "region" (last occurrence), insert --123--;

Page 15, line 10, after "negative", insert --,--;

Page 16, bottom paragraph, first line, change "base to" to --base-to-";

Page 16, bottom paragraph, line 4, after "gate", insert --126A--; after "region" (last occurrence), insert --123A--;

Page 16, bottom paragraph, line 6, after "region", insert --123A--;

Page 16, bottom paragraph, line 7, change "ro" to --for--;

Page 17, line 3, after "shield", insert --121--;

Page 17, first full paragraph, line 5, after "region", insert --17--;

Page 18, first full paragraph, line 3, after "contact", insert --11C--;

Page 18, last paragraph, line 1, change "in" to --by way of--; after "second", insert --(surface)--;

Page 18, last paragraph, line 2, change "$217_a$" to --217--; before "prior", insert --(deeper)--; after "region" (last occurrence), insert --217A--;

Page 18, last paragraph, line 3, change "as shown" to --, refer to above--;

Page 18, last paragraph, line 4, after "region", insert --11--; before "layer", insert --top gate--;

Page 19, line 2, change "region" to --body 11--;

Page 19, line 3, after "layers", insert --217, 250 respectively--;

Page 19, first full paragraph, line 3, change "region" to --body 11--;

Page 19, first full paragraph, line 4, change "region" to --first drift region 217--;

Page 19, first full paragraph, line 6, after "contact", insert

--12A--; change "region" to --body 11--;

Page 19, first full paragraph, line 7, change "drain body" to

--drain-to-body--;

Page 19, first full paragraph, line 8, before "region", insert

--first drift--;

Page 20, line 3, change "layer" to --first drift region--;

Page 20, line 4, change "layer" (first occurrence) to --first drift region--; change "layer" (last occurrence" to --region--;

Page 20, line 5, change "layer" to --region 250--;

Page 20, first full paragraph, line 2, change "drain body" to

--drain-to-body--;

Page 20, first full paragraph, line 3, after "junction", insert --15--; change "P and N-" to --P N- --;

Page 20, first full paragraph, line 4, change "P to N" to --P N--; change "N and " to --N first drift region 217 and--;

Page 20, first full paragraph, line 5, change "regions" to --body 11--; after "layer", insert --250--;

Page 20, first full paragraph, line 6, change "layer" to --first drift region--;

Page 21, line 4, change "layer" to --first drift region--;

Page 21, first full paragraph, line 2, change "layers" to --regions--; change "250" to --221--;

Page 21, last paragraph, line 2, change "250" to --221--;

Page 21, last paragraph, line 3, change "region" to --body 11--; and

Page 21, last paragraph, line 4, change "region" (last occurrence) to --first drift region 217--.

IN THE CLAIMS:

Claim 1, delete without prejudice, and substitute therefor the following new claims.

--31. A semiconductor device comprising:

a semiconductor body of a first conductivity type having a first surface;

a first semiconductor region of a second conductivity type formed in a first portion of said first surface of said semiconductor body, and defining a first PN junction with said semiconductor body;

a second semiconductor region of said first conductivity type formed in a surface portion of said first semiconductor region and defining therewith a second PN junction, said second PN junction being spaced apart from said first PN junction by material of said first semiconductor region therebetween;

a third semiconductor region of said first conductivity type formed in a second surface portion of said semiconductor body, spaced apart from said first surface portion by a third surface portion thereof;

a fourth semiconductor region of said second conductivity type formed in a first surface part of said third surface portion of said semiconductor body spaced apart from said first surface portion of said semiconductor body by a second surface part of said third surface portion thereof and defining with said semiconductor body a third PN junction, said fourth semiconductor region being connected to said first semiconductor region and being contiguous with said third semiconductor region;

a fifth semiconductor region of said first conductivity type, and having an impurity concentration greater than that of said semiconductor body, formed in said fourth semiconductor region and defining therewith a fourth PN junction, said fifth semiconductor region being contiguous with said third semiconductor region;

an insulator layer formed on said first surface of said semiconductor body; and

a gate electrode formed on said insulator layer so as to overlie said second surface part of said third surface portion of said semiconductor body and material of said first and fourth semiconductor regions, that portion of said first semiconductor region lying beneath said gate electrode serving as a channel region of said device, said gate electrode having a gate voltage applied to induce a conductive channel through said first semiconductor region therebeneath; and wherein

when said device is reverse-biased, a first depletion region extends from said fourth PN junction into said fourth semiconductor region and said semiconductor body, and a second depletion region extends from said fifth PN junction into said fifth semiconductor region and said fourth semiconductor region;

said semiconductor body having a first ON resistance in a first current flow path therethrough between said second and third semiconductor regions, and said fifth semiconductor region providing a second ON resistance in a second current flow path along the surface of said semiconductor body from said second semiconductor region through said channel and said fourth and fifth semiconductor regions to said third semiconductor region, so that said fifth semiconductor region serves to provide a current flow path in parallel with said first current flow path, thereby effectively reducing the total ON resistance of the overall current flow path between said second and third semiconductor regions.

32. A semiconductor device according to claim 31, wherein a peripheral edge of said gate electrode is aligned with a peripheral edge of said fifth semiconductor region.

33. A semiconductor device according to claim 31, wherein said fourth semiconductor region overlaps said first semiconductor region.

34. A semiconductor device according to claim 31, wherein the impurity concentration said fifth semiconductor region is such that said fifth semiconductor region is completely depleted by said second depletion region at a reverse bias less than that at which said first and second depletion regions come together within and punch through said fourth semiconductor region.

35. A semiconductor device comprising:

a semiconductor body of a first conductivity type having a first surface;

a first semiconductor region of a second conductivity type formed in a first portion of said first surface of said semiconductor body, and defining a first PN junction with said semiconductor body;

a second semiconductor region of said first conductivity type formed in a surface portion of said first semiconductor region and defining therewith a second PN junction, said second PN junction being spaced apart from said first PN junction by material of said first semiconductor region therebetween;

a third semiconductor region of said first conductivity type formed in a second surface portion of said semiconductor body, spaced apart from said first surface portion by a third surface portion thereof;

a fourth semiconductor region of said second conductivity type formed in said third surface portion of said semiconductor body and defining with said semiconductor body a third PN junction, said fourth semiconductor region being connected to said first semiconductor region and being contiguous with said first and third semiconductor regions;

a fifth semiconductor region of said first conductivity type, and having an impurity concentration greater than that of said semiconductor body, formed in said fourth semiconductor region and defining therewith a fourth PN junction, said fifth semiconductor region being contiguous with said first and third semiconductor regions;

an insulator layer formed on said first surface of said semiconductor body; and

a gate electrode formed on said insulator layer so as to overlie material of said first and fourth semiconductor regions, that portion of said first semiconductor region lying beneath said gate electrode serving as a channel region of said device, said gate electrode having a gate voltage applied to induce a conductive channel through said first semiconductor region therebeneath; and wherein

when said device is reverse-biased, a first depletion region extends from said fourth PN junction into said fourth semiconductor region and said semiconductor body, and a second depletion region extends from said fifth PN junction into said fifth semiconductor region and said fourth semiconductor region.

36. A semiconductor device according to claim 34 wherein the impurity concentration said fifth semiconductor region is such that said fifth semiconductor region is completely depleted by said second depletion region at a reverse bias less than that at which said first and second depletion regions come together within and punch through said fourth semiconductor region.

37. A semiconductor device comprising:

a semiconductor body of a first conductivity type having a first surface;

a first semiconductor region of a second conductivity type formed in a first portion of said first surface of said semiconductor body, and defining a first PN junction with said semiconductor body;

a second semiconductor region of said first conductivity type formed in a second surface portion of said semiconductor body, spaced apart from said first surface portion by a third surface portion thereof and defining a second PN junction with said semiconductor body;

a third semiconductor region of said second conductivity type formed in a first surface part of said third surface portion of said semiconductor body spaced apart from said first surface portion of said semiconductor body by a second surface part of said third surface portion thereof and defining with said semiconductor body a third PN junction, said third semiconductor region being contiguous with said second semiconductor region;

a fourth semiconductor region of said first conductivity type, and having an impurity concentration greater than that of said semiconductor body, formed in said third semiconductor region and defining therewith a fourth PN junction;

an insulator layer formed on said first surface of said semiconductor body; and

a gate electrode formed on said insulator layer so as to overlie said second surface part of said third surface portion of said semiconductor body, that portion of said semiconductor body lying beneath said gate electrode serving as a channel region of said device, said gate electrode being applied with a gate voltage for inducing a conductive channel through said channel region;

said device being reverse-biased, so that a first depletion region extends from said third PN junction into said third semiconductor region and said semiconductor body and a second depletion region extends from said fourth PN junction into said third semiconductor region and said fourth semiconductor region;

said semiconductor body having a first ON resistance in a first current flow path therethrough between said first and second semiconductor regions, and said fourth semiconductor region providing a second ON resistance, less than said first ON resistance, in a second current flow path along the surface of said semiconductor body from said first semiconductor region through said channel and said third and fourth semiconductor regions to said second semiconductor region, so that said fourth semiconductor region serves to provide a reduced resistance current flow path in parallel with said first current flow path,

thereby effectively reducing the total ON resistance of the overall current flow path between said first and second semiconductor regions; and

wherein the impurity concentration said fourth semiconductor region is such that said fourth semiconductor is completely depleted by said second depletion region at a reverse bias less than that at which said first and second depletion regions come together within and punch through said third semiconductor region.

38. A high voltage MOS transistor comprising:

a semiconductor substrate of a first conductivity type having a surface,

a pair of laterally spaced source and drain pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,

an extended drain region of the second conductivity type extending laterally each way from said drain pocket to surface-adjoining positions,

a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain pocket and the surface-adjoining positions,

said top layer of material and said substrate being subject to application of a reverse-bias voltage,

an insulating layer on the surface of the substrate and covering at least that portion between the source pocket and the nearest surface-adjoining position of the extended drain region, and

a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the source pocket and the nearest surface-adjoining position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.

39. A high voltage MOS transistor according to claim 38, wherein said extended drain region has an impurity concentration greater than $1x10^{12}$ $cm^{-2}$.

40. A high voltage MOS transistor according to claim 38, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor substrate, said ohmic contact region overlapping said top layer of material.

41. A high voltage MOS transistor comprising:

semiconductor material of a first conductivity type having a surface,

a pair of laterally spaced source and drain pockets of semiconductor material of a second conductivity type within the substrate and adjoining the surface of said semiconductor material,

an extended drain region of the second conductivity type extending laterally from said drain pocket to a surface-adjoining position,

a surface adjoining top layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain pocket and said surface-adjoining position,

said top layer of material and said semiconductor material being subject to application of a reverse-bias voltage,

an insulating layer on the surface of said semiconductor material and covering at least that portion between the source pocket and the nearest surface-adjoining position of the extended drain region, and

a gate electrode on the insulating layer and electrically isolated from a semiconductor material region thereunder containing a channel that extends laterally between the source pocket and the nearest surface-adjoining position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.

42. A high voltage MOS transistor according to claim 41, wherein said extended drain region extends in a plurality of different directions from said drain pocket to respective plural surface adjoining positions.

43. A high voltage MOS transistor according to claim 41, wherein said extended drain region surrounds said drain pocket and extends to a surrounding surface adjoining position.

44. A high voltage MOS transistor according to claim 41, wherein said drain pocket comprises a first relatively deep pocket of a first impurity concentration and a second relatively shallow pocket formed in a surface portion of said first relatively deep pocket and having a second impurity concentration greater than said first impurity concentration and providing a drain contact region.

45. A high voltage MOS transistor according to claim 41, wherein said extended drain region has an impurity concentration greater than $1x10^{12}$ $cm^{-2}$.

46. A high voltage MOS transistor according to claim 41, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor material, said ohmic contact region overlapping said top layer of material.

47. A high voltage field effect transistor device comprising:

semiconductor material of a first conductivity type having a surface;

a source region of a second conductivity type formed in a first surface portion of said semiconductor material;

a drain region of said second conductivity type formed in a second surface portion of said semiconductor material spaced apart from said first surface portion by a third surface portion therebetween;

an extended drain region of said second conductivity type extending from said drain region beneath a first portion of said third surface portion of said semiconductor material, to adjoin a second portion of said third surface portion of said semiconductor material, spaced apart from said second surface portion of said semiconductor material, by said first portion of said third surface portion of said semiconductor material;

a surface region of said first conductivity type formed in said first portion of said third surface portion of said semiconductor material;

an insulating layer disposed on said surface of said semiconductor material, so as to overlie a third portion of said third surface portion of said semiconductor material between the second portion of said third surface portion of said semiconductor material and said first surface portion of said semiconductor material; and

a gate electrode disposed on that portion of said insulating layer overlying said third portion of said third surface portion of said semiconductor material, and wherein said surface region and said semiconductor material are subject to the application of a reverse bias voltage.

48. A high voltage field effect transistor device according to claim 47, wherein said extended drain region extends laterally in a plurality of different directions from said drain region to adjoin said second portion of said third surface portion of said semiconductor material and to adjoin a fifth surface portion of said semiconductor material.

49. A high voltage field effect transistor device according to claim 47, wherein said extended drain region surrounds said drain region and extends to a surrounding surface-adjoining portion of said semiconductor material.

50. A high voltage field effect transistor device according to claim 47, wherein said drain region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration and providing a drain contact region.

51. A high voltage field effect transistor device according to claim 47, wherein said extended drain region has an impurity concentration greater than $1x10^{12}$ $cm^{-2}$.

52. A high voltage field effect transistor device according to claim 47, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor material, said ohmic contact region overlapping said surface region.

53. An integrated MOS/JFET transistor device comprising an insulated gate field effect transistor and a double-sided junction field effect transistor integrated together in semiconductor substrate which contains a source region, and a drain region formed therein, and a dual channel path formed in said semiconductor material between said source and drain regions, said dual channel path comprising an insulated gate-controlled channel region having a first conductivity type in the presence of a channel-inducing gate voltage, said insulated gate controlled channel region being contiguous with a double-sided junction channel region of said first conductivity type, and wherein said source region adjoins said insulated gate-controlled channel region and said drain region adjoins said double-sided channel region.

54. An integrated MOS/JFET transistor device according to claim 53, wherein said insulated gate-controlled channel region comprises a surface portion of said semiconductor material adjoining said source region, and wherein said double-sided junction channel region comprises an extended drain region extending laterally from said drain region beneath a top gate region to said surface portion of said semiconductor material, an underlying portion of said semiconductor material extending beneath and adjoining said extended drain region and forming a bottom gate, said top gate region and said bottom gate forming respective PN junctions with said double-sided junction channel region.

55. An integrated MOS/JFET transistor device according to claim 53, wherein said extended drain region and said double-sided junction channel region surround said drain region and extend to a surrounding surface-adjoining position.

56. An integrated MOS/JFET transistor device according to claim 53, ~~wherein said extended drain region and said double,~~ wherein said drain region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration and providing a drain contact region.

57. An integrated MOS/JFET transistor device according to claim 53, ~~wherein said extended drain region and said double,~~ further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor material, said ohmic contact region overlapping said top gate.

58. An integrated MOS/JFET transistor device according to claim 53, wherein said extended drain region has an impurity concentration greater than $1x10^{12}$ $cm^{-2}$.

59. A high voltage MOS transistor comprising:

semiconductor material of a first conductivity type having a surface;

source and drain regions of a second conductivity type adjoining spaced apart portions of the surface of said semiconductor material;

an extended drain region of said second conductivity type extending laterally from said drain region through said semiconductor material to a surface-adjoining portion of the surface of said semiconductor material;

a top gate semiconductor layer of said first conductivity type adjoining said drain region and adjoining said extended drain region along the surface of said semiconductor material to said surface-adjoining portion of the surface of said semiconductor material, said top gate semiconductor layer and said semiconductor material being subject to the application of a reverse-bias voltage;

an insulating layer on the surface of the semiconductor material and covering at least that portion of the surface of said semiconductor material between said source region and said surface-adjoining portion of said extended drain region; and

a gate electrode disposed on said insulating layer and being electrically isolated from that portion of the surface of said semiconductor material thereunder which forms a channel laterally between said source region and said surface-adjoining portion of said extended drain region, said gate electrode controlling, by field-effect, the flow of current thereunder through said channel.

60. A high voltage MOS transistor according to claim 59, wherein said extended drain region extends laterally each way from said drain region to surface-adjoining portions of the surface of said semiconductor material, and wherein said top gate semiconductor layer extends laterally in a plurality of different directions from said drain region and adjoins said extended drain region along the surface of said semiconductor material to said surface-adjoining portions of the surface of said semiconductor material.

61. A high voltage MOS transistor according to claim 59, wherein said extended drain region surrounds said drain region and extends to a surrounding surface adjoining position.

62. A high voltage MOS transistor according to claim 59, wherein said drain region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration and providing a drain contact region.

63. A high voltage MOS transistor according to claim 59, wherein said extended drain region has an impurity concentration greater than $1x10^{12}$ $cm^{-2}$.

64. A high voltage MOS transistor according to claim 59, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor material, said ohmic contact region overlapping said top gate layer.

65. A high voltage diode comprising:

semiconductor material of a first conductivity type having a surface,

a first, surface-adjoining region of a second conductivity type;

a second surface-adjoining region of said first conductivity type spaced apart from said first, surface-adjoining region;

a third region of said second conductivity type extending laterally from said first, surface-adjoining region; and

a fourth, surface-adjoining region of said first conductivity type overlying an intermediate portion of said third, laterally extending and surface-adjoining region.

66. A high voltage diode according to claim 65, wherein said third region surrounds said first, surface-adjoining region and extends to a surrounding surface adjoining position.

67. A high voltage diode according to claim 65, wherein said first region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration.

68. A high voltage diode according to claim 65, wherein said third region has an impurity concentration greater than $1x10^{12}$ $cm^{-2}$.

69. A lateral bipolar transistor having a high voltage base-collector diode comprising:

semiconductor material of a first conductivity type having a surface and forming a base of said bipolar transistor,

a first, surface-adjoining collector region of a second conductivity type forming a base-collector junction with said semiconductor material;

a second surface-adjoining base region of said first conductivity type spaced apart from said first, surface-adjoining collector region;

a third, extended collector region of said second conductivity type extending laterally from said first, surface-adjoining collector region, so that said base-collector junction extends laterally from said first, surface adjoining collector region;

a fourth, surface-adjoining region of said first conductivity type overlying an intermediate portion of said third, laterally extending and surface-adjoining extended collector region; and

a fifth, surface-adjoining emitter region of said second conductivity type formed in said second surface-adjoining base region and defining therewith an emitter-base junction.

70. A lateral bipolar transistor according to claim 69, wherein said third region surrounds said first, surface-adjoining region and extends to a surrounding surface adjoining position.

71. A lateral bipolar transistor according to claim 69, wherein said first region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration.

72. A lateral bipolar transistor according to claim 69, wherein said third, extended collector region has an impurity concentration greater than $1x10^{12}$ $cm^{-2}$.--

REMARKS

The specification has been amended to conform with the Amendment filed July 13, 1990 in parent application Serial No. 242,405.

Original claims 1-30 have been replaced by new claims 31-72. Of these newly presented claims, claims 31-37 correspond to those claims filed in the Amendments of July 13, 1990 and January 25, 1991, in parent application Serial No. 242,405, and incorporating the Amendments of the Examiner's Amendment dated February 22, 1991. New claims 38-72 embody further definitions of subject matter for which patent protection is sought.

With respect to newly added claims 38-72, to the extent that 37 C.F.R. 1.607(c) is applicable, please be advised that claim 38, although not identically copied, is considered to be generic to the invention defined in claim 1 of U.S. Patent No. 4,811,075 to Eklund. Claims 41, 47 and 59 are also considered to be generic to the invention defined in claim 1 of the patent to Eklund, 4,811,075.

U.S. Patent No. 4,823,173, of which application Serial No. 242,405, filed September 8, 1988 is a continuation-in-part, has a filing date of January 7, 1986, the present application being a continuation of application Serial No. 242,405, it is respectfully submitted that the effective filing date of the above-identified claims is the filing date of parent Patent 4,823,173, or January 7, 1986. This filing date antedates the filing date of April 24, 1987 of the above-identified Eklund patent, 4,811,075.

Early examination of the present application is earnestly solicited.

To the extent necessary, Applicants petition for an Extension of Time under 37 C.F.R. 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including Extension of Time fees, to Deposit Account No. 05-1323 (118/28508CO) and please credit any excess fees to such deposit account.

Respectfully submitted,

_____

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# United States Patent [19]

Beasom

[11] Patent Number: 5,264,719

[45] Date of Patent: Nov. 23, 1993

[54] **HIGH VOLTAGE LATERAL SEMICONDUCTOR DEVICE**

[75] Inventor: **James D. Beasom**, Melbourne Village, Fla.

[73] Assignee: **Harris Corporation**, Melbourne, Fla.

[21] Appl. No.: **705,509**

[22] Filed: **May 24, 1991**

**Related U.S. Application Data**

[63] Continuation of Ser. No. 242,405, Sep. 8, 1988, abandoned, which is a continuation-in-part of Ser. No. 831,384, Jan. 7, 1986, Pat. No. 4,823,173.

[51] **Int. Cl.**[5] ..... **H01L 29/80**

[52] **U.S. Cl.** ..... **257/335**; 257/336; 257/339

[58] **Field of Search** ..... 357/38, 55, 23.8, 46

[56] **References Cited**

U.S. PATENT DOCUMENTS

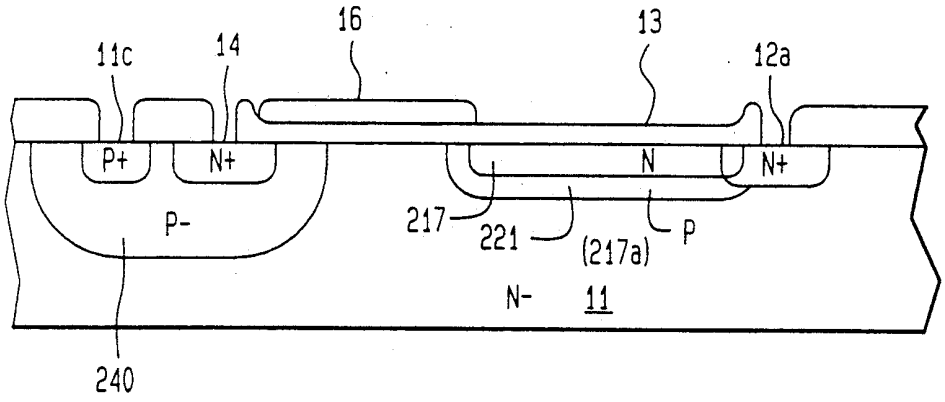
| | | | |
|---|---|---|---|
| 4,626,879 | 12/1986 | Colak | 357/23.8 |
| 4,628,341 | 12/1986 | Thomas | 357/23.8 |
| 4,811,075 | 3/1989 | Eklund et al. | 357/46 |
| 4,994,889 | 2/1991 | Takeuchi et al. | 357/55 |
| 4,994,904 | 2/1991 | Nakagawa et al. | 357/38 |

*Primary Examiner*—Rolf Hille
*Assistant Examiner*—Roy Potter
*Attorney, Agent, or Firm*—Evenson, Wands, Edwards, Lenahan & McKeown

[57] **ABSTRACT**

The present invention provides an improved lateral drift region for both bipolar and MOS devices where improved breakdown voltage and low ON resistance are desired. A top gate of the same conductivity type as the device region with which it is associated is provided along the surface of the substrate and overlying the lateral drift region. In an MOS device, the extremity of the lateral drift region curves up to the substrate surface beyond the extremity of the top gate to thereby provide contact between the JFET channel and the MOS channel.

**42 Claims, 7 Drawing Sheets**



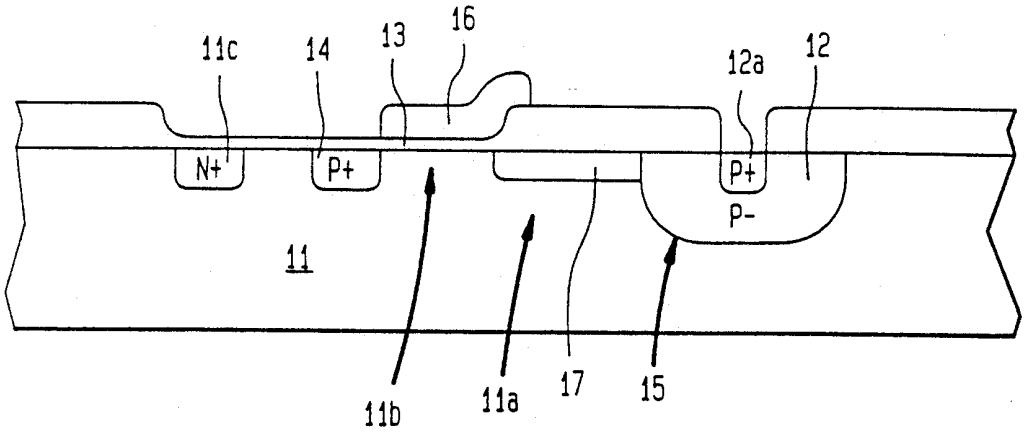



FIG. 1

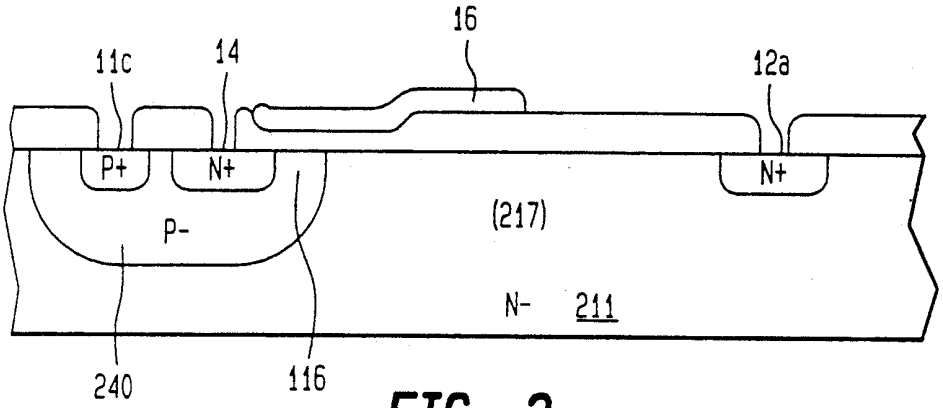



FIG. 2
(PRIOR ART)

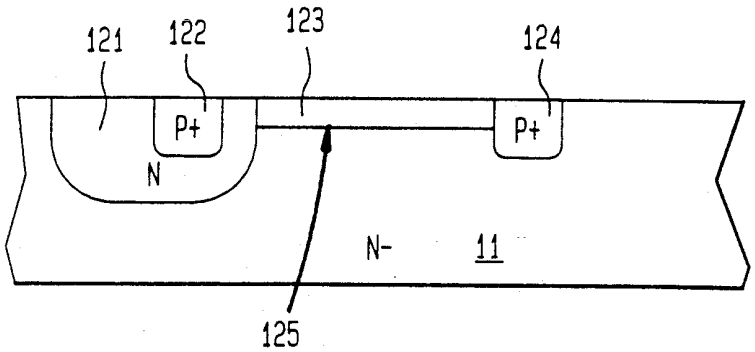



FIG. 3

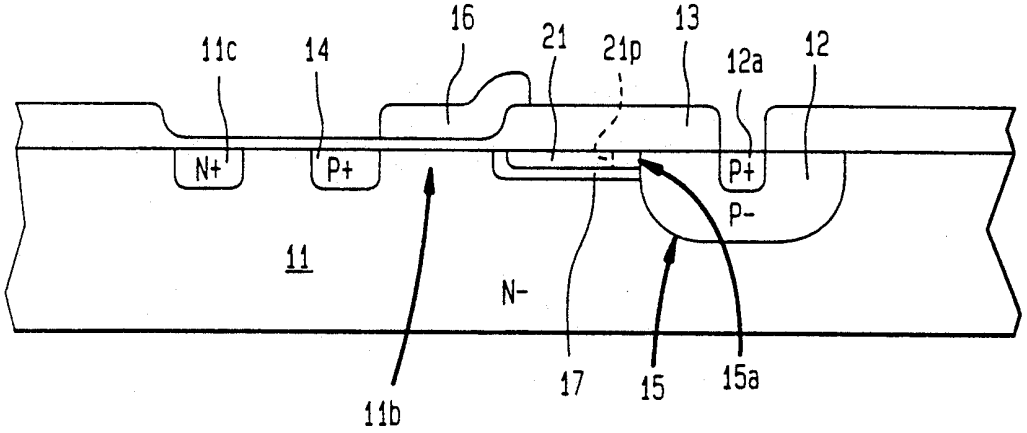

16
21
13
11c
14
21p
12a
12
N+
P+
P+
P-
11
N-
11b
17
15
15a

FIG. 4

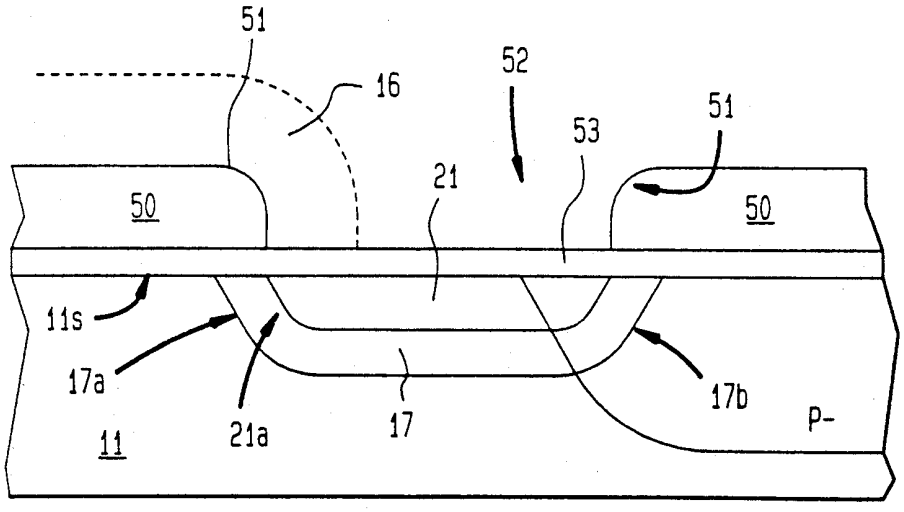

51
16
52
51
53
21
50
50
11s
17a
17b
P-
11
21a
17

FIG. 5

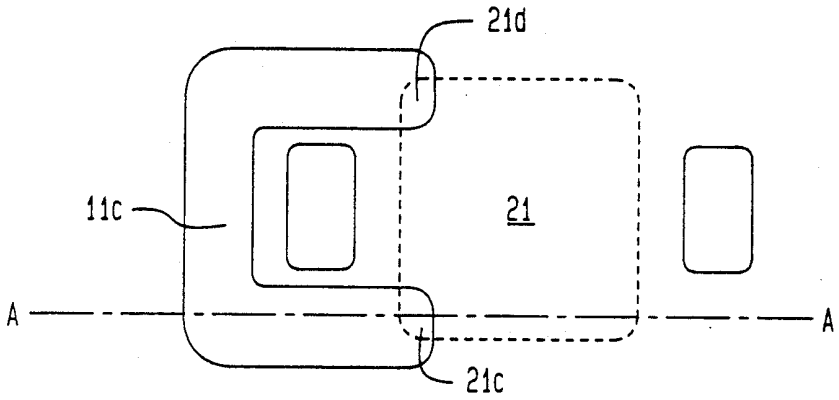



FIG. 6a

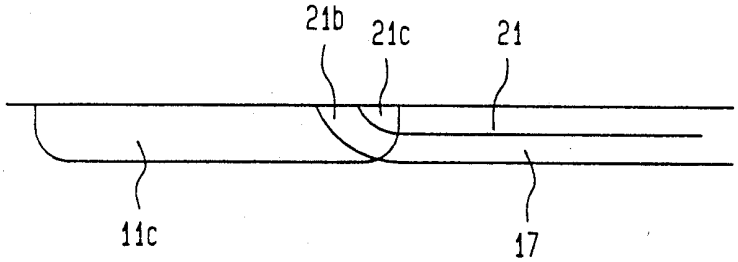



FIG. 6b

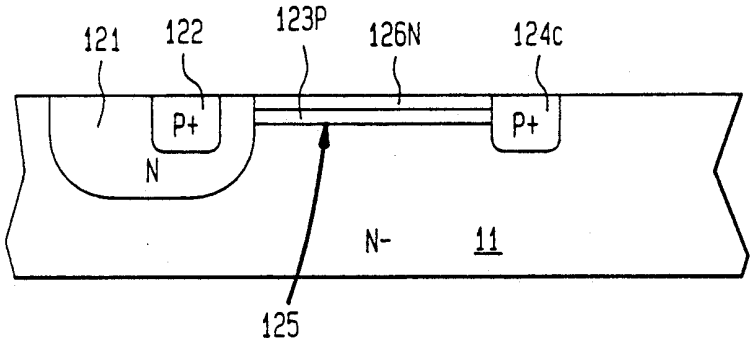

121
122
123P
126N
124c
P+
P+
N
N-
11
125

FIG. 7

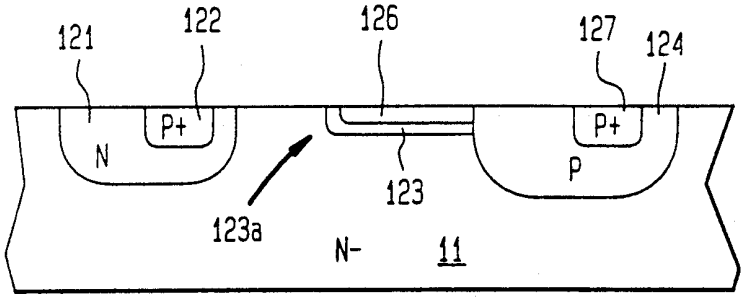

121
122
126
127
124
P+
P+
N
P
123
123a
N-
11

FIG. 8

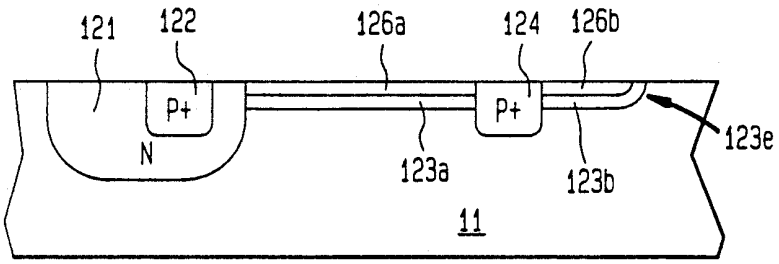

121
122
126a
124
126b
P+
P+
N
123a
123b
123e
11

FIG. 9

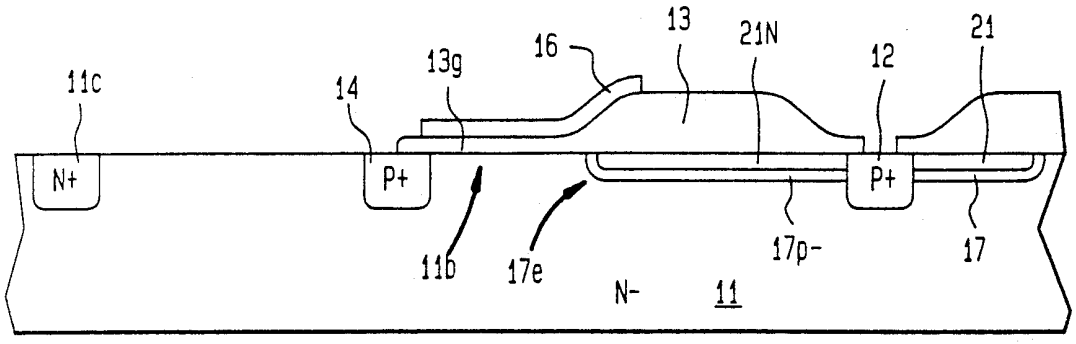

11c
14
13g
16
13
21N
12
21
N+
P+
P+
11b
17e
17p-
17
N-
11

FIG. 10

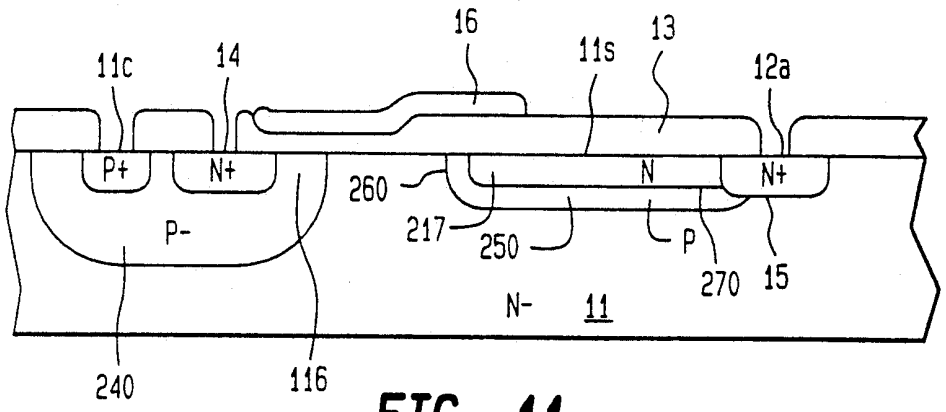

16
11s
13
11c
14
12a
P+
N+
260
N
N+
P-
217
250
P
270
15
N- 11
240
116

FIG. 11

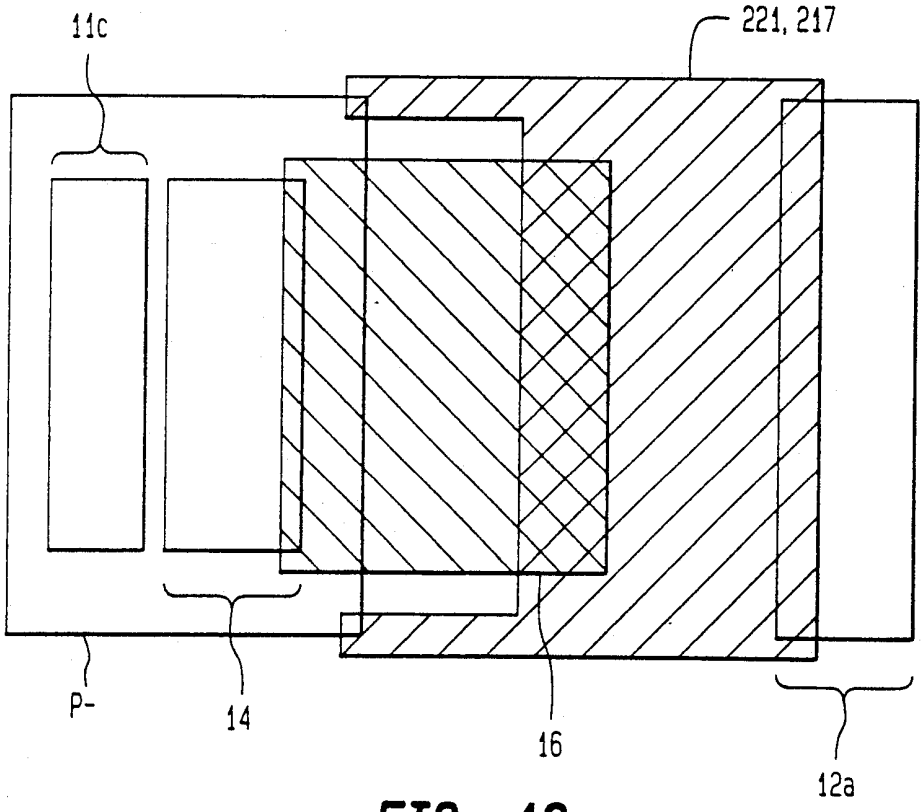

11c
221, 217
P-
14
16
12a

FIG. 12

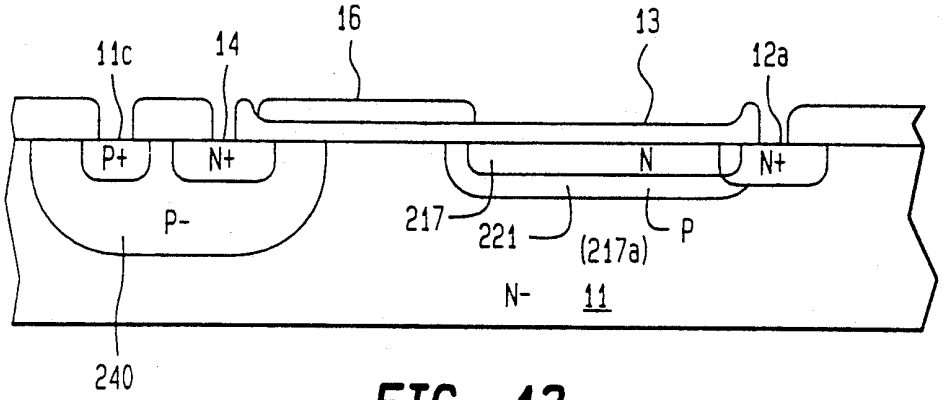

16
13
11c
14
12a
P+
N+
N
N+
P-
217
221
(217a)
P
N- 11
240

FIG. 13

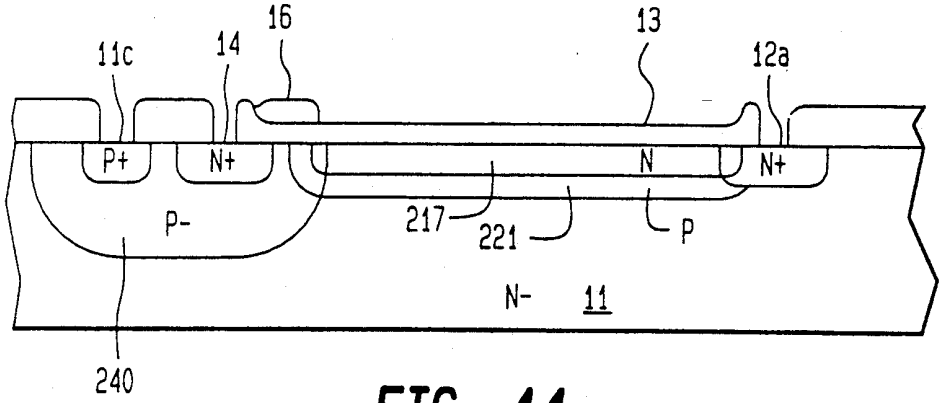

16
13
11c
14
12a
P+
N+
N
N+
P-
217
221
P
N- 11
240

FIG. 14

# HIGH VOLTAGE LATERAL SEMICONDUCTOR DEVICE

This is a continuation of application, Ser. No. 242,405, filed Sep. 8, 1988, now abandoned which, in turn, is a continuation-in-part of application, Ser. No. 831,384, filed Jan. 7, 1986, now U.S. Pat. No. 4,823,173, issued Apr. 18, 1989.

## FIELD OF THE INVENTION

The present invention relates to lateral semiconductor devices and an improved method of making lateral semiconductor devices. More specifically, the invention relates to high voltage lateral devices with reduced ON resistance and a method of making such devices.

Previous high voltage lateral devices include both MOS devices and bipolar transistors. For example, FIG. **1** illustrates a known structure which can be used as a high voltage lateral MOS device. This device is known as a lateral drift region MOS device and is dependent upon the drain-to-body junction **15** as the basic high voltage junction of the device. The drift region **17** is a P region along the top surface of the N− substrate **11** and is located so as to lie adjacent the P− drain region **12**. The drift region **17** is used to connect the high voltage drain **12** to the gate **16** and source **14**. The two contacts, drain contact $12_a$ and body contact $11_c$ are shown for completeness. In the operation of this circuit, the gate **16** and source **14** never assume large voltages relative to the body **11**. The drift region **17** serves as a JFET channel with the portion $11_a$ of body region **11** underlying the channel acting as a JFET gate. The JFET channel **17** is designed to totally deplete when the drain **12** is reverse biased to a voltage less than the voltage necessary to reach critical field in the channel-to-body depletion layer. This design preserves the effective high breakdown voltage of drain body junction **15**. Also the source **14** and gate **16** (over the gate oxide **13**) are safely shielded from the high drain body voltage by the pinched off JFET channel **17**.

The resistance of the lateral drift region JFET channel **17** is in series with the resistance of the MOS channel $11_b$, consequently the total channel resistance of the device is the sum of these two individual resistances. The JFET channel, which must be quite long to sustain high drain body voltages, is often the larger of the two resistance terms. Thus it is desirable to find ways to reduce the resistance of the drift region so that devices of a given size can be made with smaller channel resistance.

FIG. **2** illustrates a known structure which can be used as a high voltage lateral DMOS (LDMOS) device. In this device, an N+ drain contact **12A** is formed in the N− substrate **211** and an N+ source **14** and P+ body contact $11_c$ are formed in a P− body region **240**. The drift region **217** is an N− region along the top surface of the N− substrate **211** which connects the drain **12** to the gate **16** and source **14**. In this high voltage device, the N− drift region **217** must be lightly doped to obtain high body **240** to drain breakdown.

The ON resistance of the LDMOS is approximately the sum of the channel resistance and the bulk resistance in the N− drift region **217**. The lateral distance from the N+ drain **12** to the adjacent edge of the MOS channel $11_b$ underlying the gate on the P− body **240** must be large to allow space for the reverse bias depletion layer which spreads from the body-to-drain junction into the lightly doped drain. This distance, along with the high N− resistivity contribute to the high drift region resistance, which is often much greater than the channel resistance. Thus, it is desirable to reduce the drift region resistance of the LDMOS device.



FIG. **3** shows a known structure which can be used as a lateral bipolar transistor. Another illustration of such a device is contained in FIG. 7 of U.S. Pat. No. 4,283,236 issued Aug. 11, 1981. Referring to FIG. **3**, an N− substrate **11**, has an N type emitter shield **121** formed therein and P+ emitter **122** and collector **124** formed as shown. Additionally, a P− drift region **123** is provided along the surface of the substrate between the collector **124** and the emitter shield **121**. In the operation of this device, the total collector resistance is equal to the sum of the resistance across the drift region **125** plus the resistance of the P+ collector between the drift region and the collector contact. In order to provide devices of equal size having a lower collector resistance, it is desirable to find ways to reduce the resistance of the drift region.

In the operation of this device, the drift region extends the collector to the edge of the emitter shield, **121**, so that the base width is just that small distance between the adjacent edges of the emitter, **121**, and the drift region, therefore, providing improved frequency response.

At high base-collector voltages, the drift region, **123**, depletes by JFET action with the N-base, **11**, and N shield, **121**, which is part of the base, acting as gate before critical field is reached just as for the MOS of FIG. **1**. This preserves the high breakdown of the structure.

## SUMMARY OF THE INVENTION

The present invention provides a structure having a reduced channel resistance and a process capable of efficiently obtaining the structure of the invention. The reduction in channel resistance is accomplished by providing a top gate which is located between the lateral drift region of the prior art and the surface of the channel region and which may be in contact with the high voltage device region. This top gate allows the total channel doping to be increased because the top gate to channel depletion layer holds some additional channel charge when reverse biased in addition to that held by the bottom gate to channel depletion layer of the prior art structure. The ionized channel impurity atoms associated with this additional channel charge causes the reduction in channel resistance.

With respect to providing an improved LDMOS structure having a lower drift region resistance, a second drift region which is separated from the original drift region by a region of opposing conductivity is formed. The second drift region provides a conductive path which is in parallel with the original drift region thereby achieving the desired reduction in resistance. Because of the formation of the second drift region, the first enclosed drift region can now have a much higher doping than the second drift region which it replaces, while achieving the same breakdown voltage.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a cross section of a known MOS device having typical ON resistance.

FIG. **2** is a cross section of a known LDMOS device having typical ON resistance.

FIG. **3** is a cross section of a known bipolar transistor having typical collector resistance.

FIG. **4** is a cross section of an MOS device including the improved drift region and top gate of the invention.

FIG. **5** illustrates optimized process steps for obtaining the desired shape of the top gate and drift region of the invention.

FIGS. **6***a* and **6***b* are, respectively, a top view and a cutaway perspective view of the body contact extending through the top gate and drift region of the invention.

FIG. **7** is a cross section of a bipolar device made in accordance with one aspect of the invention.

FIG. **8** is a cross section of a bipolar device made in accordance with another aspect of the invention.

FIG. **9** is a cross section of a bipolar device made in accordance with a preferred aspect of the invention.

FIG. **10** is a cross section of an MOS device, including the lateral drift region and top gate of the invention, in a preferred embodiment.

FIG. **11** is a cross section of a LDMOS device made in accordance with a preferred embodiment of the invention.

FIG. **12** is a top view of the LDMOS device of FIG. **11**.

FIG. **13** is a cross section of a LDMOS device made in accordance with another preferred embodiment of the invention.

FIG. **14** is a cross section of a LDMOS device made in accordance with still another preferred embodiment of the invention.

## DETAILED DESCRIPTION OF THE INVENTION

The present invention is described herein with reference to the drawings for both MOS and bipolar applications. FIG. **4** shows an MOS device where $P^+$ drain contact $12_a$ is formed in $P^-$ type drain **12**, $P^+$ source **14** is formed in the $N^-$ body **11** and $N^+$ body contact $11_c$ is provided in the $N^+$ body **11**. The MOS channel region $11_b$ is in the $N^-$ body **11** below the MOS gate **16**. The N type top gate **21** is provided along the surface $11_s$ of the body **11** above the P type drift region **17** which acts as a JFET channel. The lateral edge or peripheral edge of both the top gate **21** and drift region **17** extend to the drain-to-body junction **15** and preferably terminate at the junction **15**. It is noted that situations may exist where the doping level in the top gate may be sufficiently high so as to render it desirable to provide a shorter top gate having a lateral extension which stops short of contacting the junction **15**. In this case care should be taken to insure that any nondepleted portion of the top gate does not result in a breakdown of the top gate-to-drift region junction 17A. Proper doping of the top gate **21** will generally be a sufficient preventative step. Dashed line $21_p$ designates the peripheral edge of top gate **21** in an embodiment where the top gate does not extend all the way to the junction **15**.

The structure of FIG. **4** provides reduced ON resistance in the JFET channel **17** relative to the prior art lateral drift MOS device as shown in FIG. **1**. The reduction in ON resistance is accomplished by providing a structure which can accommodate increased drift region doping without suffering from reduced body-to-drain breakdown. This is possible because of the provision of the top gate **21**. The top gate-to-channel depletion layer which holds some channel charge when reverse biased, is in addition to the channel charge held by the bottom gate to channel depletion layer of the prior art. This additional channel charge, in the form of ionized channel impurity atoms, causes the reduction in channel resistance. It is possible to provide more than twice the doping level previously acceptable due to the additional ability to hold channel change. Thus, for a drift region **17** having a doping of $1\times10^{12}$ boron atoms per square centimeter in a bottom gate arrangement, the present invention will permit $2\times10^{12}$ boron atoms per square centimeter. Thus, the ON resistance will be only half the ON resistance of the prior arrangement.

In order to optimize performance of the structure of the invention, the top gate **21** must be designed differently than an ordinary JFET gate. Top gate **21** should become totally depleted at a body-to-drain voltage of less than the breakdown voltage of the top gate-to-drain junction **15**. Since top gate **21** is connected to body **11** (as shown in FIGS. **6A**, **6B** to be described below), the voltage at the top gate-to-drain junction $15_a$ will equal the voltage of the body-to-drain junction **15** voltage and the top gate-to-drain breakdown voltage should be greater than the voltage at which top gate **21** becomes totally depleted. Additionally, the top gate **21** must totally deplete before the body **11** to channel **17** depletion layer reaches the top gate **21** to channel **17** depletion layer to thereby assure that a large top gate **21** to drain **12** voltage is not developed by punch-through action from the body **11**. An ordinary JFET gate never totally depletes regardless of operating conditions.

In addition to the above described characteristics of the device of the invention, it is also necessary to insure that the channel of the JFET drift region **17** contacts the inversion layer MOS surface channel. This can be accomplished as shown in FIG. **5** where an implant mask **50** having a tapered edge **51** is provided over the body **11**. An implant aperture **52** is provided in mask **50** at the location where the P drift region **17** and N top gate **21** are to be formed. The aperture **52** is shown as exposing the protective oxide **53**. Ion implantation is not substantially affected by the oxide **53** due to the oxide thickness of only about 0.1–0.2 micrometers, yet the oxide provides surface passivation for the underlying body **11**.

The drift region **17** is ion implanted and, because of the graduated thickness of the implant mask **50** (along the edge **51**), the depth of the implanted drift region **17** is graduated or tapered. In the illustration, a fairly good rounding of the drift region **17** occurs at the peripheral edges or extremeties $17_a$, $17_b$ of the region **17**. The curved extremity $17_a$ is of interest because at this location the channel of the JFET drift region **17** contacts the surface $11_s$ of body **11** beyond the end $21_a$ of top gate **21** and is desirably beneath the gate **16** of the MOS device. The top gate **21** may be ion-implanted using the implant mask **50** but at an energy level which results in a shallower implantation. This tapered profile, particularly if curved, provides improved performance.

In a variation of this method, a diffusion process can be used to bring the JFET channel into contact with the surface of body **11**, and hence insure that the JFET channel **17** will contact the inversion layer MOS surface channel (lateral drift region **17** and top gate **21** are diffused after initial introduction by ion implant). The doping levels and diffusion times are chosen such that the extremity $17_a$ of JFET channel **17** diffuses beyond the end $21_a$ of the top gate **21** and so that the end $17_a$ reaches the surface $11_s$ of body **11**. In practice, this approach can be facilitated by choosing a top gate dop-

ant which has a lower diffusion coefficient than that of the drift region dopant.

The formation of the drift region **17** and top gate **21** may be conveniently carried out by forming a mask over the gate oxide which is present in a lateral MOS application. The MOS gate may be utilized as one delineating edge of the implant for the drift region and top gate and a thick oxide portion surrounding a thinner oxide portion may form the remainder of the implant mask. The thinner oxide portion shall be located such that it extends from beneath the MOS gate to the drain and preferably overlaps the drain. The implant mask **50** illustrated in FIG. **5** is shown as having thin oxide portion **53** being surrounded by the implant mask **50**. If the MOS gate **16** shown in dashed lines were used as a portion of the mask **50**, the edge of the drift region and top gate would be self-aligned with the MOS gate as shown in dashed lines. Then, when diffused, the drift region will extend laterally to a point beneath the MOS gate, while the top gate **21** may be formed such that there is little or no lateral overlap with the MOS gate. The extent of lateral diffusion of the top gate is dependent upon the dopant material and processing temperatures following top gate implant. It is noted that there is a separation between the drift region and the source. This separation zone is the location where the MOS channel is located.

The top gate **21** will perform as previously described if it is tied to the body **11**. Thus, the top gate **21** and the body which operates as the bottom gate of the JFET channel will be at equal potential. According to the invention, this may be accomplished in a particularly effective manner if the drift region **17** is widened to overlap with the body contact region $11_c$. This is shown in FIG. **6***a* which shows the overlapping of the top gate **21** and the body contact $11_c$ at the overlap regions $21_c$, $21_d$. In order for this arrangement to be effective, it is necessary that the body contact $11_c$ have a higher dopant concentration than the JFET channel (or drift region) **17**, as shown in FIG. **6***b* to insure that the body contact $11_c$ forms a continuous region horizontally and/or vertically through the JFET channel and to the body region **11** from the top gate, **21**.

FIG. **6***b* shows a cross section of the structure of FIG. **6***a* taken along dashed line A—A. The body **11** is provided with body contact $11_c$ which is located such that the top gate **21** and drift region **17** can be conveniently extended to overlap the body contact $11_c$. The depth of body contact $11_c$ may be made greater than the depth of region **17** such that a portion of the body contact $11_c$ extends below region **17** and provides contact with the body **11**. This arrangement provides a contact portion $21_c$ where the top gate **21** is in contact with body contact $11_c$. Thus, as long as the body contact doping concentration in region $21_b$ is sufficiently high to overcome the opposite doping in region **17**, then a good connection of uniform conductivity type will be provided between the top gate **21** and the body **11**, via contact region $11_c$. It is also noted that the body contact $11_c$ extends laterally beyond the end of both of the top gate **21** and the drift region **17**. The lateral extension of the contact $11_c$ will also provide a structure which results in a good connection of uniform conductivity type from the top gate **21** to the body **11**, again, provided that the doping of body contact $11_c$ converts region $21_b$.

Another area where the present invention finds application is in lateral bipolar transistors which employ a lateral drift region. The known structure of FIG. **3** may be improved by providing an N type top gate **126** as shown in FIG. **7**. In this arrangement the N type gate **126** extends from the collector **124** to the emitter shield **121** along the surface of body **11**. The operation of this device is enhanced by the same phenomenon as the lateral drift region of the previously described MOS device. As the base **11** becomes positive relative to the collector **124**, the top gate-to-drift region depletion layer facilitates pinch-off of the drift region **123**. However, as the base **11** becomes more negative, the top gate **126** contributes additional surface exposure to the drift region **123** and further enhances carrier transportation.

FIG. **8** shows an improvement over the arrangement shown in FIG. **7**. In FIG. **8** the drift region **123** does not extend all the way over to the emitter shield **121**. The curved end $123_a$ of the drift region **123** contacts the top surface of body **11**. It is noted that in this arrangement, the emitter shield **121** may be omitted.

An additional improvement shown in FIG. **8** is the use of a deep diffusion to form the collector **124** resulting in a significantly increased breakdown voltage. The deep diffusion step may be the same step used for forming the emitter, in which case the collector **124** shown in FIG. **7** would be deeper, or a separate collector implant and diffusion step may be employed and the collector contact **127** may then be formed simultaneously with the formation of the emitter **122**. This improvement in junction breakdown voltage is equally obtainable, for example, at the body to drain junction in the MOS devices described previously.

A further extension of the invention which may be used to increase base-to-collector breakdown voltage for a PNP device is shown in FIG. **9**. In addition to the provision of the N type top gate $126_a$ over the P− drift region $123_a$, the top gate **126A** and drift region **123A** are enlarged to surround the collector **124** and a curved edge $123_e$ is provided at the periphery of the enlarged portion $123_b$ of the drift region **123A**. This enlarged portion is designated by reference numerals $123_b$ for the drift region and $126_b$ for the top gate. The collector **124** to base **11** breakdown voltage is increased relative to alternative arrangements because of mitigation of the breakdown reduction due to the junction curvature. The top gate $126_a$ extends to the emitter shield **121** as does the drift region $123_a$. The P+ emitter **122** is formed in the N+ type emitter shield **121**.

FIG. **10** illustrates an extension of the invention with respect to a P channel MOS device similar to the improvement described with respect to the bipolar device shown in FIG. **9**. For the MOS device, the drain **12** is surrounded by the P− drift region **17** and N type top gate **21**. Around the entire periphery of the drift region **17** there is a curved portion $17_e$ which rounds up to the surface of the N− substrate **11** to insure that the JFET channel in the drift region **17** contacts the MOS channel $11_b$ under the MOS gate **16**. The drift region **17** extends outward from the entire perimeter of the drain **12**. This arrangement mitigates the breakdown reduction due to junction curvature. The P+ source **14** and N+ body contact $11_c$ are shown as is the dielectric **13** which serves as the gate oxide $13_g$ beneath the MOS gate **16**.

In both the arrangements shown in FIG. **9** and FIG. **10**, the planar diode breakdown improvement created by the drift region acting as a surface layer of the same conductivity type as the collector in FIG. **9** and drain in FIG. **10** and extending out from the perimeter of the collector and drain can be implemented by a single series of process steps. According to the invention, a

common set of process steps produces both a suitable breakdown improvement layer and an improved drift region. The breakdown improvement layer is a two layer component.

A further extension of the invention is illustrated in FIG. **11** which shows an LDMOS device where $N^+$ drain contact $12_a$ is formed in an $N^-$ type substrate and an $N^+$ source **14** and $P^+$ body contact $11_c$ are formed in a $P^-$ type body region **240**. The DMOS channel region $11_b$ is in the $P^-$ body **240** below the DMOS gate **16**. The N type first drift region **217** is provided along the surface $11_s$ of the substrate **11** above a $P^-$ type separation region **250**. A second drift region $217_a$ exists in the substrate **11** underneath the $P^-$ type separation region. The lateral edge of both the first drift region **217** and the separation region **250** extend from the gate **16** to the $N^+$ drain contact $12_a$.

The structure in FIG. **11** provides reduced ON resistance by way of the second (surface) drift region $217_a$ relative to the (deeper) prior art lateral first drift region $217_a$ device, refer to above in FIG. **2**. To illustrate this, consider an example in which the $N^-$ region **11** has a doping of $1\times10^{14}$ ions $cm^{-3}$. The top gate layer **217** has an integrated doping of about $1\times10^{12}$ ions $cm^{-2}$ and is preferably not more than two microns thick while maintaining full breakdown. The thickness of the N and P layers **217**, **250** together is preferably less than ten microns and can be less than one micron. The same integrated doping in the $N^-$ body **11** requires a thickness of 100 microns. Thus, the N and P layers **217**, **250** respectively consume only a small fraction of the $N^-$ thickness required to provide doping equal to that portion of the N layer of the prior art device.

The lateral spacing between the drain contact $12_a$ and the channel $11_b$ in the device described above would be approximately 30 microns. In such a device, even if a full 100 micron thick $N^-$ body **11** were provided, it would have a higher resistance than the $N^-$ first drift region **217** provided according to the invention. This is because the average path length of current flowing from the drain contact **12A** down through the thick $N^-$ body **11** and back up to the surface edge of the channel at the drain-to-body junction would be greater than the direct path through the $N^-$ first drift region.

Maximum breakdown is achieved in the invention by providing doping densities of the N and P layers **217**, **250** such that they become totally depleted before breakdown is reached at any point along the junctions which they form with adjoining regions and before breakdown is reached at the junction between them. To insure that this occurs, the N region **217** should have an integrated doping not exceeding approximately $1\times10^{12}$ ions $cm^{-2}$ and the P region **250** should have a higher integrated doping not exceeding about 1.5 to $2\times10^{12}$ ions $cm^{-2}$.

To insure proper depletion of the P and N regions **250**, **217**, they must have the proper voltages applied. The N layer bias is achieved by connecting the N first drift region **217** to the higher concentration $N^+$ drain contact $12_a$ by overlapping the N first drift region **217** and drain contact $12_a$. The P region **250** bias is achieved by overlapping the P region **250** with the $P^-$ body **240** at least at one end of the channel, thereby applying the body voltage to the P layer **250**. This is illustrated in FIG. **12**.

With this structure and choice of doping levels, the desired results are achieved. When a reverse bias voltage is applied to the drain-to-body junction **15**, the same reverse bias appears on both the $PN^-$ junction **260** and the PN junction **270**. Depletion layers spread up into the N first drift region **217** and and down into the $N^-$ body **11** from the P layer **250**. In a preferred embodiment, the P and N first drift region dopings are chosen such that the N layer **217** becomes totally depleted at a lower voltage than that at which the P layer **250** becomes totally depleted. This insures that no residual undepleted portion of the N layer **217** is present which could reduce breakdown voltage.

As a result of the invention, the improved DMOS device provides a reduced resistance current path in the drain which does not depend on the $N^-$ doping. This allows the $N^-$ doping to be reduced to achieve a desired breakdown voltage with good manufacturing margin, while maintaining desirable low drift region resistance. In a multi-device process which includes LDMOS devices, the $N^-$ region can be adjusted to achieve the desired characteristics of one or more of the other device types, while the N first drift region **217** sets the drift region **217** resistance of the LDMOS.

Another embodiment of the DMOS invention is illustrated in FIG. **13**, where the N and P regions **217**, **221** are self-aligned to the gate **16** by using the gate **16** as a mask. An advantage of this structure is that N and P regions can be defined by the uncovered thin oxide area which extends from gate edge to overlap the drain contact. This embodiment requires no explicit mask step to delineate the location where the N and P regions are formed.

Still another embodiment, as illustrated in FIG. **14**, provides no gap between the $P^-$ body **240** and the P region **221** adjacent to the channel edge. The absence of the gap prevents current from flowing in the $N^-$ body **11**; so the entire drift region current path is in the N first drift region **217**. Elimination of the gap also allows the device structure to be made smaller. As with the other structure, the N and P regions may be self-aligned to the gate edge, as illustrated in FIG. **14**, or not self-aligned. They may also be covered by thick or thin oxide as a design option.

A preferred feature of the present invention provides that the body or substrate regions **11** shown in the FIGS. **3**, **4**, **6**, **7**, **8**, **9**, **11**, **13** and **14** are designed to be dielectrically or self-isolated regions. In contrast with the typical RESERF type of devices in which the bottom isolation junction plays a central role in the action of the device, the present invention contemplates that the isolation junction does not contribute to the depletion of the drift or top gate regions which are taught to be totally depleted. Prior art RESERF devices such as that described in U.S. Pat. No. 4,300,150 to Colak always require the substrate to be part of such depletion whereby the substrate must assume the most negative voltage in the device because of its role as one side of the isolation junction. As a result of this bias on the substrate or body region, the prior art RESERF type devices are susceptible to punch through from the device region through the epitaxial layer to the substrate. As a result of the present invention not having the substrate as part of the depletion mechanism, the invention can more effectively provide high voltage protection while not increasing the resistance of the channel path. Although the figures illustrate a nonisolating structure or self-isolated structure, it is understood that the invention applies equally well to dielectrically or junction isolated substrates.

While the present invention has been described with respect to several preferred manners of implementing the invention, it is to be understood that the claims appended hereto are intended to cover the invention in its broadest sense and are not to be limited to the specific implementations disclosed.

What is claimed is:

**1**. A semiconductor device comprising:

a semiconductor body of a first conductivity type having a first surface;

a first semiconductor region of a second conductivity type formed in a first portion of said first surface of said semiconductor body, and defining a first PN junction with said semiconductor body;

a second semiconductor region of said first conductivity type formed in a surface portion of said first semiconductor region and defining therewith a second PN junction, said second PN junction being spaced apart from said first PN junction by material of said first semiconductor region therebetween;

a third semiconductor region of said first conductivity type formed in a second surface portion of said semiconductor body, spaced apart from said first surface portion by a third surface portion thereof;

a fourth semiconductor region of said second conductivity type formed in a first surface part of said third surface portion of said semiconductor body spaced apart from said first surface portion of said semiconductor body by a second surface part of said third surface portion thereof and defining with said semiconductor body a third PN junction, said fourth semiconductor region being connected to said first semiconductor region and being contiguous with said third semiconductor region;

a fifth semiconductor region of said first conductivity type, and having an impurity concentration greater than that of said semiconductor body, formed in said fourth semiconductor region and defining therewith a fourth PN junction, said fifth semiconductor region being contiguous with said third semiconductor region;

an insulator layer formed on said first surface of said semiconductor body; and

a gate electrode formed on said insulator layer so as to overlie said second surface part of said third surface portion of said semiconductor body and material of said first and fourth semiconductor regions, that portion of said first semiconductor region lying beneath said gate electrode serving as a channel region of said device, said gate electrode having a gate voltage applied to induce a conductive channel through said first semiconductor region therebeneath; and wherein

when said device is reverse-biased, a first depletion region extends from said fourth PN junction into said fourth semiconductor region and said semiconductor body, and a second depletion region extends from said fifth PN junction into said fifth semiconductor region and said fourth semiconductor region;

said semiconductor body having a first ON resistance in a first current flow path therethrough between said second and third semiconductor regions, and said fifth semiconductor region providing a second ON resistance in a second current flow path along the surface of said semiconductor body from said second semiconductor region through said channel and said fourth and fifth semiconductor regions to said third semiconductor region, so that said fifth semiconductor region serves to provide a current flow path in parallel with said first current flow path, thereby effectively reducing the total ON resistance of the overall current flow path between said second and third semiconductor regions.

**2**. A semiconductor device according to claim **1**, wherein a peripheral edge of said gate electrode is aligned with a peripheral edge of said fifth semiconductor region.

**3**. A semiconductor device according to claim **1**, wherein said fourth semiconductor region overlaps said first semiconductor region.

**4**. A semiconductor device according to claim **1**, wherein the impurity concentration said fifth semiconductor region is such that said fifth semiconductor region is completely depleted by said second depletion region at a reverse bias less than that at which said first and second depletion regions come together within and punch through said fourth semiconductor region.

**5**. A semiconductor device comprising:

a semiconductor body of a first conductivity type having a first surface;

a first semiconductor region of a second conductivity type formed in a first portion of said first surface of said semiconductor body, and defining a first PN junction with said semiconductor body;

a second semiconductor region of said first conductivity type formed in a surface portion of said first semiconductor region and defining therewith a second PN junction, said second PN junction being spaced apart from said first PN junction by material of said first semiconductor region therebetween;

a third semiconductor region of said first conductivity type formed in a second surface portion of said semiconductor body, spaced apart from said first surface portion by a third surface portion thereof;

a fourth semiconductor region of said second conductivity type formed in said third surface portion of said semiconductor body and defining with said semiconductor body a third PN junction, said fourth semiconductor region being connected to said first semiconductor region and being contiguous with said first and third semiconductor regions;

a fifth semiconductor region of said first conductivity type, and having an impurity concentration greater than that of said semiconductor body, formed in said fourth semiconductor region and defining therewith a fourth PN junction, said fifth semiconductor region being contiguous with said first and third semiconductor regions;

an insulator layer formed on said first surface of said semiconductor body; and

a gate electrode formed on said insulator layer so as to overlie material of said first and fourth semiconductor regions, that portion of said first semiconductor region lying beneath said gate electrode serving as a channel region of said device, said gate electrode having a gate voltage applied to induce a conductive channel through said first semiconductor region therebeneath; and wherein

when said device is reverse-biased, a first depletion region extends from said fourth PN junction into said fourth semiconductor region and said semiconductor body, and a second depletion region extends from said fifth PN junction into said fifth semicon-

ductor region and said fourth semiconductor region.

6. A semiconductor device according to claim 5, wherein the impurity concentration said fifth semiconductor region is such that said fifth semiconductor region is completely depleted by said second depletion region at a reverse bias less than that at which said first and second depletion regions come together within and punch through said fourth semiconductor region.

7. A semiconductor device comprising:

a semiconductor body of a first conductivity type having a first surface;

a first semiconductor region of a second conductivity type formed in a first portion of said first surface of said semiconductor body, and defining a first PN junction with said semiconductor body;

a second semiconductor region of said second conductivity type formed in a second surface portion of said semiconductor body, spaced apart from said first surface portion by a third surface portion thereof and defining a second PN junction with said semiconductor body;

a third semiconductor region of said second conductivity type formed in a first surface part of said third surface portion of said semiconductor body spaced apart from said first surface portion of said semiconductor body by a second surface part of said third surface portion thereof and defining with said semiconductor body a third PN junction, said third semiconductor region being contiguous with said second semiconductor region;

a fourth semiconductor region of said first conductivity type, and having an impurity concentration greater than that of said semiconductor body, formed in said third semiconductor region and defining therewith a fourth PN junction;

an insulating layer formed on said first surface of said semiconductor body; and

a gate electrode formed on said insulator layer so as to overlie said second surface part of said third surface portion of said semiconductor body, that portion of said semiconductor body lying beneath said gate electrode serving as a channel region of said device, said gate electrode being applied with a gate voltage for inducing a conductive channel through said channel region;

said device being reverse-biased, so that a first depletion region extends from said third PN junction into said third semiconductor region and said semiconductor body and a second depletion region extends from said fourth PN junction into said third semiconductor region and said fourth semiconductor region;

said semiconductor body having a first ON resistance in a first current flow path therethrough between said first and second semiconductor regions, and said fourth semiconductor region providing a second ON resistance, less than said first ON resistance, in a second current flow path along the surface of said semiconductor body from said first semiconductor region through said channel and said third and fourth semiconductor regions to said second semiconductor region, so that said fourth semiconductor region serves to provide a reduced resistance current flow path in parallel with said first current flow path, thereby effectively reducing the total ON resistance of the overall current flow path between said first and second semiconductor regions; and

wherein the impurity concentration said fourth semiconductor region is such that said fourth semiconductor is completely depleted by said second depletion region at a reverse bias less than that at which said first and second depletion regions come together within and punch through said third semiconductor region.

8. A high voltage MOS transistor comprising:

a semiconductor substrate of a first conductivity type having a surface,

a pair of laterally spaced source and drain pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,

an extended drain region of the second conductivity type extending laterally each way from said drain pocket to surface-adjoining positions,

a surface adjoining, top layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain pocket and the surface-adjoining positions,

said top layer of material and said substrate being subject to application of a reverse-bias voltage,

an insulating layer on the surface of the substrate and covering at least that portion between the source pocket and the nearest surface-adjoining position of the extended drain region, and

a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the source pocket and the nearest surface-adjoining position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.

9. A high voltage MOS transistor according to claim 8, wherein said extended drain region has an impurity concentration greater than $1 \times 10^{12}$ cm$^{-2}$.

10. A high voltage MOS transistor according to claim 8, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor subscrate, said ohmic contact region overlapping said top layer of material.

11. A high voltage MOS transistor comprising:

semiconductor material of a first conductivity type having a surface,

a pair of laterally spaced source and drain pockets of semiconductor material of a second conductivity type within the substrate and adjoining the surface of said semiconductor material,

an extended drain region of the second conductivity type extending laterally from said drain pocket to a surface-adjoining position,

a surface adjoining top layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain pocket and said surface-adjoining position,

said top layer of material and said semiconductor material being subject to application of a reverse-bias voltage,

an insulating layer on the surface of said semiconductor material and covering at least that portion between the source pocket and the nearest surface-adjoining position of the extended drain region, and

a gate electrode on the insulating layer and electrically isolated from a semiconductor material re-

gion thereunder containing a channel that extends laterally between the source pocket and the nearest surface-adjoining position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.

**12**. A high voltage MOS transistor according to claim **11**, wherein said extended drain region extends in a plurality of different directions from said drain pocket to respective plural surface adjoining positions.

**13**. A high voltage MOS transistor according to claim **11**, wherein said extended drain region surrounds said drain pocket and extends to a surrounding surface adjoining position.

**14**. A high voltage MOS transistor according to claim **11**, wherein said drain pocket comprises a first relatively deep pocket of a first impurity concentration and a second relatively shallow pocket formed in a surface portion of said first relatively deep pocket and having a second impurity concentration greater than said first impurity concentration and providing a drain contact region.

**15**. A high voltage MOS transistor according to claim **11**, wherein said extended drain region has an impurity concentration greater than $1\times10^{12}$ $cm^{-2}$.

**16**. A high voltage MOS transistor according to claim **11**, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor material, said ohmic contact region overlapping said top layer of material.

**17**. A high voltage field effect transistor device comprising:

semiconductor material of a first conductivity type having a surface;

a source region of a second conductivity type formed in a first surface portion of said semiconductor material;

a drain region of said second conductivity type formed in a second surface portion of said semiconductor material spaced apart from said first surface portion by a third surface portion therebetween;

an extended drain region of said second conductivity type extending from said drain region beneath a first portion of said third surface portion of said semiconductor material, to adjoin a second portion of said third surface portion of said semiconductor material, spaced apart from said said second surface portion of said semiconductor material, by said first portion of said third surface portion of said semiconductor material;

a surface region of said first conductivity type formed in said first portion of said third surface portion of said semiconductor material;

an insulating layer disposed on said surface of said semiconductor material, so as to overlie a third portion of said third surface portion of said semiconductor material between the second portion of said third surface portion of said semiconductor material and said first surface portion of said semiconductor material; and

a gate electrode disposed on that portion of said insulating layer overlying said third portion of said third surface portion of said semiconductor material, and wherein said surface region and said semiconductor material are subject to the application of a reverse bias voltage.

**18**. A high voltage field effect transistor device according to claim **17**, wherein said extended drain region extends laterally in a plurality of different directions from said drain region to adjoin said second portion of said third surface portion of said semiconductor material and to adjoin a fifth surface portion of said semiconductor material.

**19**. A high voltage field effect transistor device according to claim **17**, wherein said extended drain region surrounds said drain region and extends to a surrounding surface-adjoining portion of said semiconductor material.

**20**. A high voltage field effect transistor device according to claim **17**, wherein said drain region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration and providing a drain contact region.

**21**. A high voltage field effect transistor device according to claim **17**, wherein said extended drain region has an impurity concentration greater than $1\times10^{12}$ $cm^{-2}$.

**22**. A high voltage field effect transistor device according to claim **17**, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor material, said ohmic contact region overlapping said surface region.

**23**. An integrated MOS/JFET transistor device comprising an insulated gate field effect transistor and a double-sided junction field effect transistor integrated together in semiconductor substrate which contains a source region, and a drain region, and a dual channel path formed in said semiconductor material between said source and drain regions, said dual channel path comprising an insulated gate-controlled channel region having a first conductivity type in the presence of a channel-inducing gate voltage, said insulated gate controlled channel region being contiguous with a double-sided junction channel region of said first conductivity type, and wherein said source region adjoins said insulated gate-controlled channel region and said drain region adjoins said double-sided channel region.

**24**. An integrated MOS/JFET transistor device according to claim **23**, wherein said insulated gate-controlled channel region comprises a surface portion of said semiconductor material adjoining said source region, and wherein said double-sided junction channel region comprises an extended drain region extending laterally from said drain region beneath a top gate region to said surface portion of said semiconductor material, an underlying portion of said semiconductor material extending beneath and adjoining said extended drain region and forming a bottom gate, said top gate region and said bottom gate forming respective PN junctions with said double-sided junction channel region.

**25**. An integrated MOS/JFET transistor device according to claim **23**, wherein said extended drain region and said double-sided junction channel region surround said drain region and extend to a surrounding surface-adjoining position.

**26**. An integrated MOS/JFET transistor device according to claim **23**, wherein said extended drain region and said double, wherein said drain region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than

said first impurity concentration and providing a drain contact region.

27. An integrated MOS/JFET transistor device according to claim 23, wherein said extended drain region and said double, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor material, said ohmic contact region overlapping said top gate.

28. An integrated MOS/JFET transistor device according to claim 23, wherein said extended drain region has an impurity concentration greater than $1\times10^{12}$ $cm^{-2}$.

29. A high voltage MOS transistor comprising:

semiconductor material of a first conductivity type having a surface;

source and drain regions of a second conductivity type adjoining spaced apart portions of the surface of said semiconductor material;

an extended drain region of said second conductivity type extending laterally from said drain region through said semiconductor material to a surface-adjoining portion of the surface of said semiconductor material;

a top gate semiconductor layer of said first conductivity type adjoining said drain region and adjoining said extended drain region along the surface of said semiconductor material to said surface-adjoining portion of the surface of said semiconductor material, said top gate semiconductor layer and said semiconductor material being subject to the application of a reverse-bias voltage;

an insulating layer on the surface of the semiconductor material and covering at least that portion of the surface of said semiconductor material between said source region and said surface-adjoining portion of said extended drain region; and

a gate electrode disposed on said insulating layer and being electrically isolated from that portion of the surface of said semiconductor material thereunder which forms a channel laterally between said source region and said surface-adjoining portion of said extended drain region, said gate electrode controlling, by field-effect, the flow of current thereunder through said channel.

30. A high voltage MOS transistor according to claim 29, wherein said extended drain region extends laterally each way from said drain region to surface-adjoining portions of the surface of said semiconductor material, and wherein said top gate semiconductor layer extends laterally in a plurality of different directions from said drain region and adjoins said extended drain region along the surface of said semiconductor material to said surface-adjoining portions of the surface of said semiconductor material.

31. A high voltage MOS transistor according to claim 29, wherein said extended drain region surrounds said drain region and extends to a surrounding surface adjoining position.

32. A high voltage MOS transistor according to claim 29, wherein said drain region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration and providing a drain contact region.

33. A high voltage MOS transistor according to claim 29, wherein said extended drain region has an impurity concentration greater than $1\times10^{12}$ $cm^{-2}$.

34. A high voltage MOS transistor according to claim 29, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor material, said ohmic contact region overlapping said top gate layer.

35. A high voltage diode comprising:

semiconductor material of a first conductivity type having a surface,

a first, surface-adjoining region of a second conductivity type;

a second surface-adjoining region of said first conductivity type spaced apart from said first, surface-adjoining region;

a third region of said second conductivity type extending laterally from said first, surface-adjoining region; and

a fourth, surface-adjoining region of said first conductivity type overlying an intermediate portion of said third, laterally extending and surface-adjoining region.

36. A high voltage diode according to claim 35, wherein said third region surrounds said first, surface-adjoining region and extends to a surrounding surface adjoining position.

37. A high voltage diode according to claim 35, wherein said first region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration.

38. A high voltage diode according to claim 35, wherein said third region has an impurity concentration greater than $1\times10^{12}$ $cm^{-2}$.

39. A lateral bipolar transistor having a high voltage base-collector diode comprising:

semiconductor material of a first conductivity type having a surface and forming a base of said bipolar transistor,

a first, surface-adjoining collector region of a second conductivity type forming a base-collector junction with said semiconductor material;

a second surface-adjoining base region of said first conductivity type spaced apart from said first, surface-adjoining collector region;

a third, extended collector region of said second conductivity type extending laterally from said first, surface-adjoining collector region, so that said base-collector junction extends laterally from said first, surface adjoining collector region;

a fourth, surface-adjoining region of said first conductivity type overlying an intermediate portion of said third, laterally extending and surface-adjoining extended collector region; and

a fifth, surface-adjoining emitter region of said second conductivity type formed in said second surface-adjoining base region and defining therewith an emitter-base junction.

40. A lateral bipolar transistor according to claim 39, wherein said third region surrounds said first, surface-adjoining region and extends to a surrounding surface adjoining position.

41. A lateral bipolar transistor according to claim 39, wherein said first region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration.

42. A lateral bipolar transistor according to claim 39, wherein said third, extended collector region has an impurity concentration greater than $1\times10^{12}$ $cm^{-2}$.

* * * * *

# United States Patent [19]

**Eklund**

[11] **Patent Number: 4,811,075**

[45] **Date of Patent: Mar. 7, 1989**


[54] **HIGH VOLTAGE MOS TRANSISTORS**


[75] Inventor: **Klas H. Eklund**, Los Gatos, Calif.

[73] Assignee: **Power Integrations, Inc.**, Mountain View, Calif.



[21] Appl. No.: **41,994**

[22] Filed: **Apr. 24, 1987**

[51] **Int. Cl.**[4] ..... **H01L 27/02**; H01L 29/78; H01L 29/80

[52] **U.S. Cl.** ..... **357/46**; 357/22; 357/23.4; 357/23.8

[58] **Field of Search** ..... 357/23.8, 23.4, 46, 357/22



[56] **References Cited**

U.S. PATENT DOCUMENTS

| | | | |
|---|---|---|---|
| 4,626,879 | 12/1986 | Colak | 357/23.8 |
| 4,628,341 | 12/1986 | Thomas | 357/23.8 |

OTHER PUBLICATIONS

Sze, *Physics of Semiconductor Devices* Wiley & Sons N.Y. c. 1981 pp. 431–438, 486–491.



*Primary Examiner*—Andrew J. James

*Assistant Examiner*—Jerome Jackson

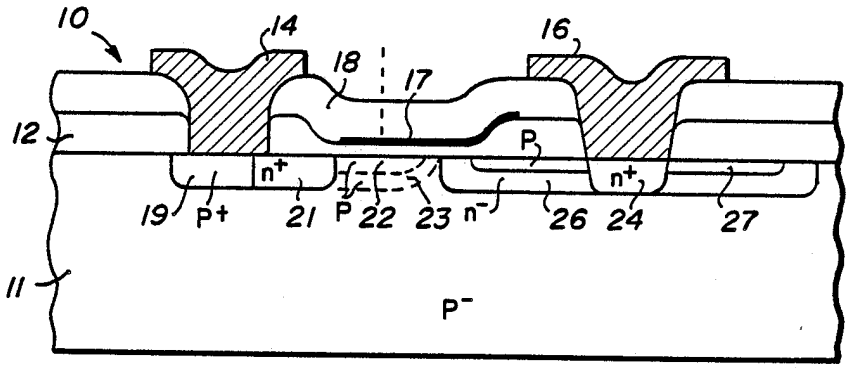
*Attorney, Agent, or Firm*—Thomas E. Schatzel



[57] **ABSTRACT**

An insulated-gate, field-effect transistor and a double-sided, junction-gate field-effect transistor are connected in series on the same chip to form a high-voltage MOS transistor. An extended drain region is formed on top of a substrate of opposite conductivity-type material. A top layer of material having a conductivity-type opposite that of the extended drain and similar to that of the substrate is provided by ion-implantation through the same mask window as the extended drain region. This top layer covers only an intermediate portion of the extended drain which has ends contacting a silicon dioxide layer thereabove. The top layer is either connected to the substrate or left floating. Current flow through the extended drain region can be controlled by the substrate and the top layer, which act as gates providing field-effects for pinching off the extended drain region therebetween. A complementary pair of such high-voltage MOS transistors having opposite conductivity-type are provided on the same chip.


**7 Claims, 2 Drawing Sheets**



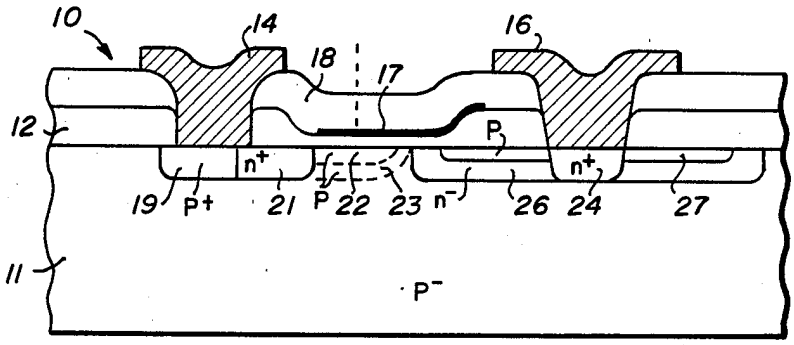



Fig_1

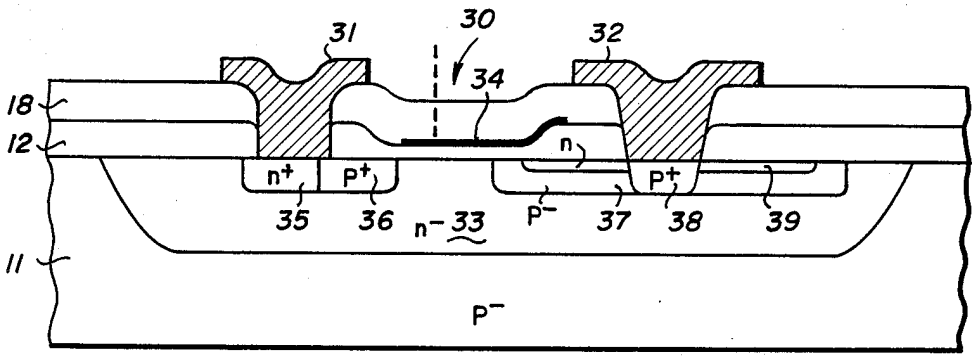



Fig_2

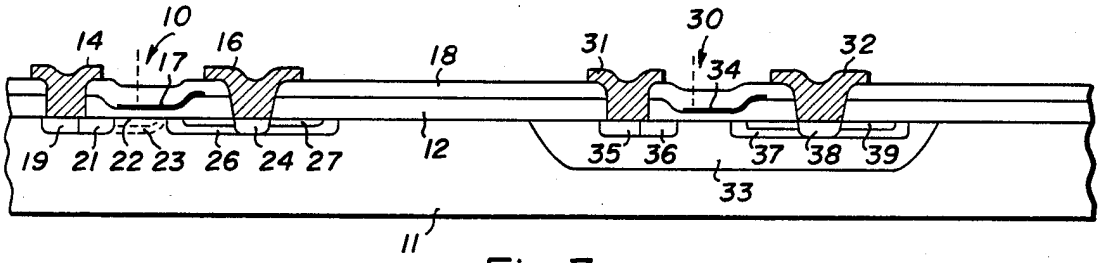



Fig_3

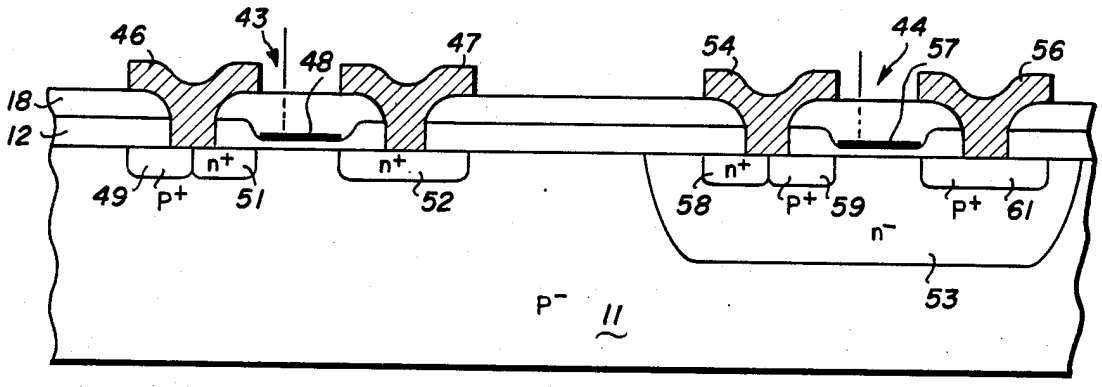

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Fig_4

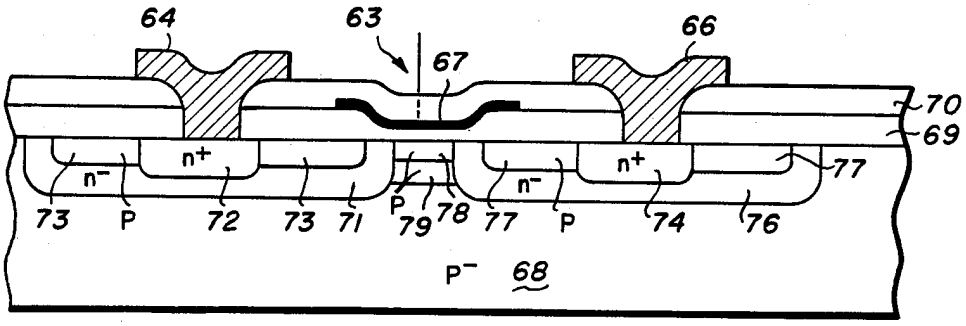
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Fig_5

# HIGH VOLTAGE MOS TRANSISTORS

## BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to high voltage metal-oxide semiconductor (MOS) transistors of the field-effect type. More specifically, the transistors can be made as either discrete or integrated devices of either n-channel or p-channel conductivity. The integrated devices can easily be combined with low voltage control logic on the same chip. Further devices of opposite conductivity can be combined in a complementary manner on the same chip.

2. Description of the Prior Art

Self isolation technology is used for making high voltage MOS devices, particularly integrated high voltage devices in combination with low voltage control logic on the same chip. The voltage is sustained by an offset gate, as a lightly doped extended drain region is used. Such devices can be considered as an IGFET or MOSFET in series with a single sided JFET. Two of such high voltage devices having opposite conductivity types can be used as a complementary pair on the same chip, with the device having an extended p-type drain being imbedded in an n-well in a p-substrate.

The voltage capability of such high voltage devices is determined by the doping of the substrate, the length of the extended drain region and the net number of charges therein. For optimum performance, the net number of charges should be around $1 \times 10^{12}/cm^2$. Such devices have been used for making display drivers in the one hundred to two hundred volt range, but the current capabilities of the devices are poor. The main advantage is that low voltage control logic easily can be combined on the same chip. For these devices, a general figure of merit can be determined by the product of $R_{on}xA$ (where $R_{on}$ is the on-resistance in the linear region and A is the area taken up by the device). For an n-channel device in the voltage range of two hundred fifty to three hundred volts, $R_{on}xA$ is typically 10–15 $\Omega$ mm$^2$. A discrete vertical D-MOS device in the same voltage range has a figure of merit of 3 $\Omega$ mm$^2$, but is much more difficult to combine with low voltage control logic on the same chip. Thus, the application of these high voltage devices is restricted to current level below 100 mA, such as display drivers. Even such drivers are more costly due to poor area efficiency of the high voltage devices.

## SUMMARY OF THE PRESENT INVENTION

An object of the present invention is to provide a more efficient high voltage MOS transistor.

Another object of the invention is to provide a high voltage MOS transistor that is compatible with five volt logic.

A further object of the invention is to provide a three hundred volt n-channel device with a figure of merit, $R_{on}$ x A, of about 2.0 $\Omega$ mm$^2$,

Briefly, the present invention includes an insulated gate, field-effect transistor (IGFET or MOSFET) and a double-sided junction gate field-effect transistor (JFET) connected in series on the same chip to form a high voltage MOS transistor. In a preferred embodiment of the invention, a complementary pair of such high voltage MOS transistors having opposite conductivity type are provided on the same chip.



Advantages of the invention include more efficient high voltage MOS transistors, compatibility with five volt logic, and for an n-channel device, voltage capability of three hundred volts with a figure of merit, $R_{on}$ x A, of about 2.0 $\Omega$ mm$^2$.

These and other objects and advantages of the present invention will no doubt become obvious to those of ordinary skill in the art after having read the following detailed description of the preferred embodiments which are illustrated in the various drawing figures.

## IN THE DRAWINGS

FIG. **1** is a diagrammatic view of a high voltage MOS transistor of the n-channel type embodying the present invention.

FIG. **2** is a diagrammatic view of a high voltage MOS transistor of the p-channel type embodying the present invention.

FIG. **3** is a diagrammatic view of the transistors shown in FIGS. **1** and **2** forming a complementary pair on the same chip.

FIG. **4** is a diagrammatic view of low voltage, C-MOS implemented devices that can be combined on the same chip with the complementary pair of high voltage MOS transistors shown in FIG. **3**.

FIG. **5** is a diagrammatic view of a symmetric high-voltage n-channel device wherein the source region and the drain region are similar.

## DESCRIPTION OF THE PREFERRED EMBODIMENT

Looking now at FIG. **1**, an n-channel type, high voltage MOS transistor, indicated generally by reference numeral **10**, is formed on a p-substrate **11** covered by a silicon dioxide layer **12**. A metal source contact **14** and a metal drain contact **16** extend through the silicon dioxide layer to the substrate. A polysilicon gate **17** is positioned between the source contact and the drain contact at a location where the silicon dioxide layer is very thin so that the gate is slightly offset and insulated from the substrate. The polysilicon gate is the gate electrode, and an insulation layer **18** covers the gate and the silicon dioxide layer.

Beneath the source contact **14**, a pocket **19** of $p^+$ material and a pocket **21** of $n^+$ material are diffused into the $p^-$ substrate **11**. The pocket **21** extends from beneath the source contact to the gate **17**. Beneath the gate is a threshold voltage implant **22** of p-type material for adjusting the threshold voltage and a punch through implant **23** of p-type material for avoiding punch through voltage breakdown. Beneath the drain contact **16**, a pocket **24** of $n^+$ material is diffused into the substrate. An extended drain region **26** of n-material is formed by diffusion or ion implantation on top of the p-substrate, and extends from beneath gate **17** to the pocket **24** and a similar distance to the opposite side of the pocket. A top layer **27** of p- material is provided by ion-implantation through the same mask window as the extended drain region to cover an intermediate portion thereof, while the end portions of the drain region are uncovered to contact the silicon dioxide layer **12**. The top layer is either connected to the substrate or left floating.

The gate **17** controls by field-effect the current flow thereunder laterally through the p-type material to the n-type material in the extended drain region **26**. Further flow through the extended drain region can be controlled by the substrate **11** and the top layer **27**, which

act as gates providing field-effects for pinching off the extended drain region therebetween. Thus, the transistor **10** can be considered as an insulated gate, field-effect transistor (IGFET or MOSFET) connected in series with a double-sided, junction-gate field-effect transistor (JFET). While the insulated gate, field-effect transistor shown is a conventional MOS type, it should be understood that it could also be a lateral D-MOS or a depletion MOS type.

By adding the top layer **27** over the extended drain region **26** and connecting this top layer to the substrate **11**, the net number of charges in the extended drain region can be increased from $1\times10^{12}/cm^2$ to around $2\times10^{12}/cm^2$, or approximately double. This drastically reduces the on-resistance of the transistor **10**. The pinch off voltage of the extended drain region can be reduced from typically around forty volts to below ten volts. Thus, a conventional short channel, thin gate oxide MOS transistors can be used as the series transistor instead of a D-MOS device. This results in the following benefits. First, the threshold voltage of a conventional MOS transistor is typically much lower than for a D-MOS device (0.7 volts compared to two four volts for the D-MOS device) and thus, is directly compatible with five volt logic. The D-MOS device usually requires an additional power supply of ten to fifteen volts for driving the gate. Second, the conventional MOS transistor has less on resistance and thus, further reduces the total on resistance.

As the p-type top layer **27** can be made very shallow with a depth of one micron or less, the doping density in that layer will be in the range of $5\times10^{16}$–$1\times10^{17}/cm^3$. At doping levels above $10^{16}/cm^3$, the mobility starts to degrade and a decrease in mobility will increase the critical electrical field for breakdown, thus giving a higher breakdown voltage for fixed geometry. The number of charges in the top layer is around $1\times10^{12}/cm^2$ and to first order approximation independent of depth.

The combined benefits of the above features result in a voltage capability of three hundred volts with a figure of merit, $R_{on}$ x A, of about 2.0 Ω $mm^2$ for the transistor **10**. Currently used integrated MOS transistors have a figure of merit of about 10–15 Ω $mm^2$, while the best discrete vertical D-MOS devices on the market in a similar voltage range have a figure of merit of 3–4 Ω $mm^2$.

With reference to FIG. **2**, a p-channel type, high voltage MOS transistor is indicated generally by reference numeral **30**. Since the layers of substrate, silicon dioxide, and insulation for this transistor are similar to those previously described for transistor **10**, they will be given like reference numerals. A p-substrate **11** is covered by a silicon dioxide layer **12** and an insulation layer **18**. A metal source contact **31** and a metal drain contact **32** extend through the insulation layer and the silicon dioxide layer to an n-well **33** that is embedded in the substrate. A polysilicon gate **34**, which is an electrode, is positioned between the source contact and the drain contact at a location where the silicon dioxide layer is very thin so that the gate is slightly offset and insulated from the n-well. The gate and the silicon dioxide layer are covered by the insulation layer **18**.

A pocket **35** of $n^+$ type material and a pocket **36** of $p^+$ type material are provided in the n-well **33** beneath the metal source contact **31**. The pocket **36** extends to the gate **34**. An extended drain region **37** of p-type material is formed in the n-well and extends from beneath the gate to a pocket **38** located beneath the drain contact **32**, and the extended drain region continues a similar distance on the opposite side of the drain contact. A top layer **39** of n-material is provided by ion-implantation through the same window of the mask as the extended drain region to cover an intermediate portion thereof. The end portions of the extended drain region are uncovered so as to contact the silicon dioxide layer **12**. The top layer is either connected to the n-well or left floating.

The gate **34** controls by field-effect the current flow thereunder laterally through the n-type material to the p-type material in the extended drain region **37**. Further flow through the extended drain region can be controlled by the n-well **33** and the top layer **39**, which act as gates providing field-effects for pinching off the extended drain region therebetween. Thus, the transistor **30** can be considered as an insulated-gate field-effect transistor (IGFET or MOSFET) connected in series with a double-sided, junction-gate field-effect transistor (JFET). The n-well under the extended drain region has to be depleted before breakdown occurs between the $p^+$ drain contact pocket **38** and the n-well.

Looking now at FIG. **3**, an n-channel transistor **10**, similar to that shown in FIG. **1**, and a p-channel transistor **30**, similar to that shown in FIG. **2**, are shown as a complementary pair on the same substrate **11** and isolated from each other. Since the details of each transistor has been previously described with reference to FIGS. **1** and **2**, no further description is considered necessary.

As shown in FIG. **4**, low voltage, C-MOS implemented devices **43** and **44** can be combined on the same p-substrate **11** as the high voltage devices **10** and **30**, shown in FIG. **3**. These low voltage devices enable low voltage logic and analog function to control the high voltage devices. The device **43** is an n-channel type having a source contact **46**, a drain contact **47** and a polysilicon gate **48**. A $p^+$ pocket **49** and an $n^+$ pocket **51** are provided in the $p^-$ substrate beneath the source contact. The $n^+$ pocket extends to beneath the gate. An $n^+$ pocket **52** is provided beneath the drain contact. The gate **48** is insulated from the substrate by the silicon dioxide layer **12**, but the gate controls the current flow through the substrate between pockets **51** and **52**. The gate is covered by the insulation layer **18**. An n-well **53** is provided in the substrate to accommodate the low voltage, p-channel device **44**. This device includes a source contact **54**, a drain contact **56** and a polysilicon gate **57**. An $n^+$ pocket **58** and a $p^+$ pocket **59** are provided in the n-well beneath the source contact and a $p^+$ pocket **61** is provided in the n-well beneath the drain contact. The gate **57** is insulated from the n-well and extends thereabove between pockets **59** and **61**.

It should be noted that the term "substrate" refers to the physical material on which a microcircuit is fabricated. If a transistor is fabricated on a well of n or p type material within a primary substrate of opposite type material, the well material can be considered a secondary substrate. Similarly, if a transistor is fabricated on an epitaxial layer or spi-island that merely supports and insulates the transistor, the epitaxial layer or epi-island can be considered a secondary substrate. An epi-island is a portion of an epitaxial layer of one conductivity type that is isolated from the remaining portion of the epitaxial layer by diffusion pockets of an opposite conductivity type. When complimentary transistors are formed on the same chip, the well in which one compli-

mentary transistor is embedded is formed by the same diffusion as the extended drain region for the other transistor.

FIG. 5 shows a symmetrical n-channel device 63 having a source contact 64 and a drain contact 66. A polysilicon gate 67 is insulated from a substrate 68 by a silicon dioxide layer 69 and the gate is covered by an insulation layer 20. An n-type extended source region 71 is provided beneath the source contact and an $n^+$ type pocket 72. A top layer 73 of p-type material is positioned over an intermediate portion of the extended source region, while the end portions of the extended source region contact the silicon dixode layer thereabove. Beneath the drain contact is an $n^+$ type pocket 74 and an n-type extended drain region 76. A top layer 73 of p-type material is positioned over an intermediate portion of the extended drain region and end portions of the extended drain region contact the silicon dioxide layer. An implant 78 of the p-type material is provided under the gate 67 between the extended source region and the extended drain region for sustaining the threshold voltage. A similar implant 79 for sustaining the punch-through voltage is provided beneath the implant 78. Since the symmetrical channel device has both an extended source an an extended drain, the source can sustain the same high potential as the drain. A symmetric p-channel device could be made in a similar way using opposite conductivity type materials.

From the foregoing description, it will be seen that an efficient, high voltage MOS transistor has been provided. This transistor is compatible with five volt logic which easily can be integrated on the same chip. The transistor has a voltage capability of three hundred volts for an n-channel device, and has a figure of merit, $R_{on} \times A$, of about 2.0 $\Omega mm^2$. The transistor is formed by an insulated-gate field-effect transistor and a double-sided junction-gate field-effect transistor connected in series on the same chip. These transistors can be made as either discrete devices or integrated devices of either n-channel or p-channel conductivity. The integrated devices can be easily combined with low voltage control logic on the same chip. Further devices of opposite conductivity can be combined in a complementary manner on the same chip.

Although the present invention has been described in terms of the presently preferred embodiment, it is to be understood that such disclosure is not to be interpreted as limiting. Various alterations and modifications will no doubt become apparent to those of ordinary skill in the art after having read the above disclosure. Accordingly, it is intended that the appended claims be interpreted as covering all alterations and modifications as fall within the true spirit and scope of the invention.

I claim:

1. A high voltage MOS transistor comprising:
- a semiconductor substrate of a first conductivity type having a surface
- a pair of laterally spaced pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,
- a source contact connected to one pocket,
- a drain contact connected to the other pocket,
- an extended drain region of the second conductivity type extending laterally each way from the drain contact pocket to surface-adjoining positions,
- a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjoining positions,
- said top layer of material and said substrate being subject to application of a reverse-bias voltage,
- an insulating layer on the surface of the substrate and covering at least that portion between the source contact pocket and the nearest surface-adjoining position of the extended drain region, and
- a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the source contact pocket and the nearest surface-adjoining position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.

2. The high-voltage MOS transistor of claim 1 wherein,

said top layer has a depth of one micron or less.

3. The high-voltage MOS transistor of claim 1 wherein,

said top layer has a doping density higher than $5 \times 10^{16}/cm^3$ so that the mobility starts to degrade.

4. The high voltage MOS transistor of claim 1 having one channel conductivity type in combination with a complementary high voltage MOS transistor of an opposite channel conductivity type combined on the same chip and isolated from each other.

5. The high voltage MOS transistor of claim 1 combined on the same chip with a low voltage CMOS implemented device.

6. The combination of claim 5 further including,
- a complementary high voltage MOS transistor, and
- a complementary low voltage CMOS implemented device on the same chip and isolated from each other.

7. A high voltage MOS transistor comprising:
- a semiconductor substrate of a first conductivity type having a surface,
- a pair of laterally spaced pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,
- a source contact connected to one pocket,
- an extended source region of the second conductivity type extending laterally each way from the source contact pocket to surface-adjoining positions,
- a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended source region between the surface-adjoining positions,
- said top layer and said substrate being subject to application of a reverse-bias voltage,
- a drain contact connected to the other pocket,
- an extended drain region of the second conductivity type extending laterally each way from the drain contact pocket to surface-adjoining positions,
- a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjoining positions,
- said top layer of material and said substrate being subject to application of a reverse-bias voltage,
- an insulating layer on the surface of the substrate and covering at least that portion between the nearest surface-adjoining positions of the extended source region and the extended drain region, and
- a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the nearest surface-adjoining positions of the extended source region and the extended drain region, said gate electrode controlling by field-effect the current flow thereunder through the channel.

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# United States Patent [19]

**Eklund**

[11] **Patent Number: 4,811,075**

[45] **Date of Patent: Mar. 7, 1989**


[54] **HIGH VOLTAGE MOS TRANSISTORS**


[75] Inventor: **Klas H. Eklund**, Los Gatos, Calif.

[73] Assignee: **Power Integrations, Inc.**, Mountain View, Calif.



[21] Appl. No.: **41,994**

[22] Filed: **Apr. 24, 1987**

[51] **Int. Cl.**[4] ..... **H01L 27/02**; H01L 29/78; H01L 29/80

[52] **U.S. Cl.** ..... **357/46**; 357/22; 357/23.4; 357/23.8

[58] **Field of Search** ..... 357/23.8, 23.4, 46, 357/22



[56] **References Cited**

U.S. PATENT DOCUMENTS

| | | | |
|---|---|---|---|
| 4,626,879 | 12/1986 | Colak | 357/23.8 |
| 4,628,341 | 12/1986 | Thomas | 357/23.8 |

OTHER PUBLICATIONS

Sze, *Physics of Semiconductor Devices* Wiley & Sons N.Y. c. 1981 pp. 431–438, 486–491.



*Primary Examiner*—Andrew J. James

*Assistant Examiner*—Jerome Jackson

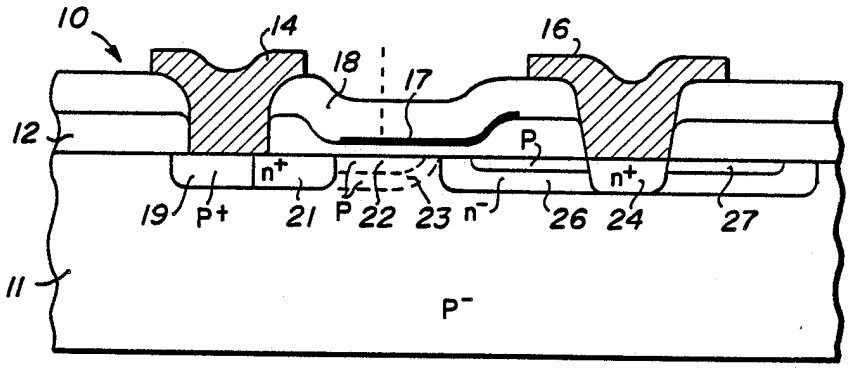
*Attorney, Agent, or Firm*—Thomas E. Schatzel



[57] **ABSTRACT**

An insulated-gate, field-effect transistor and a double-sided, junction-gate field-effect transistor are connected in series on the same chip to form a high-voltage MOS transistor. An extended drain region is formed on top of a substrate of opposite conductivity-type material. A top layer of material having a conductivity-type opposite that of the extended drain and similar to that of the substrate is provided by ion-implantation through the same mask window as the extended drain region. This top layer covers only an intermediate portion of the extended drain which has ends contacting a silicon dioxide layer thereabove. The top layer is either connected to the substrate or left floating. Current flow through the extended drain region can be controlled by the substrate and the top layer, which act as gates providing field-effects for pinching off the extended drain region therebetween. A complementary pair of such high-voltage MOS transistors having opposite conductivity-type are provided on the same chip.


**7 Claims, 2 Drawing Sheets**



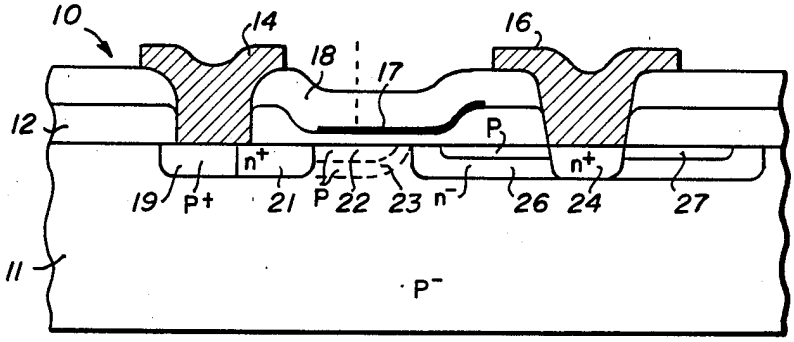



Fig_1

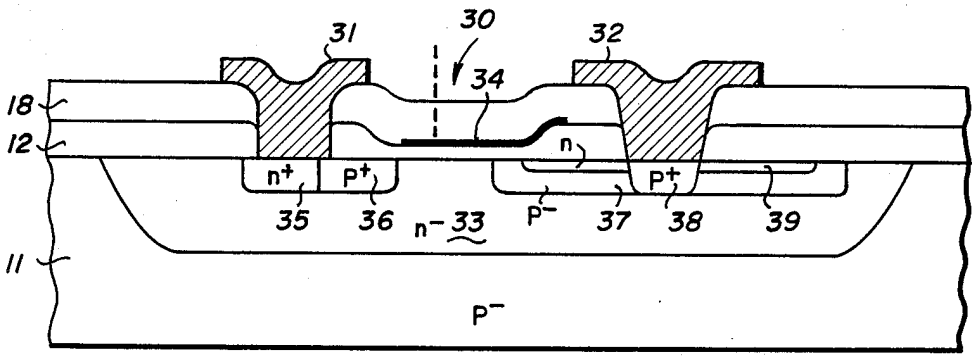



Fig_2

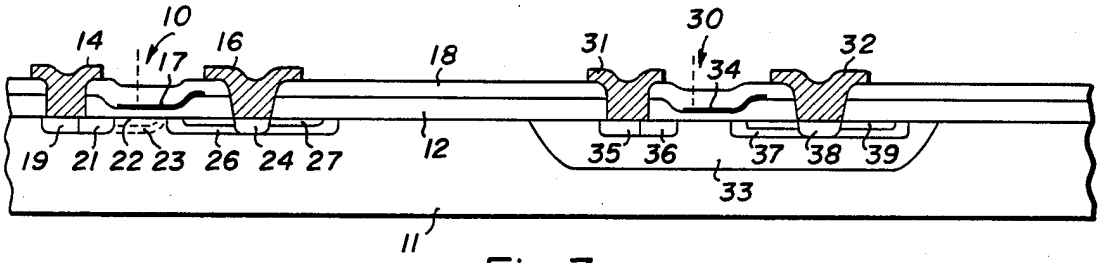



Fig_3

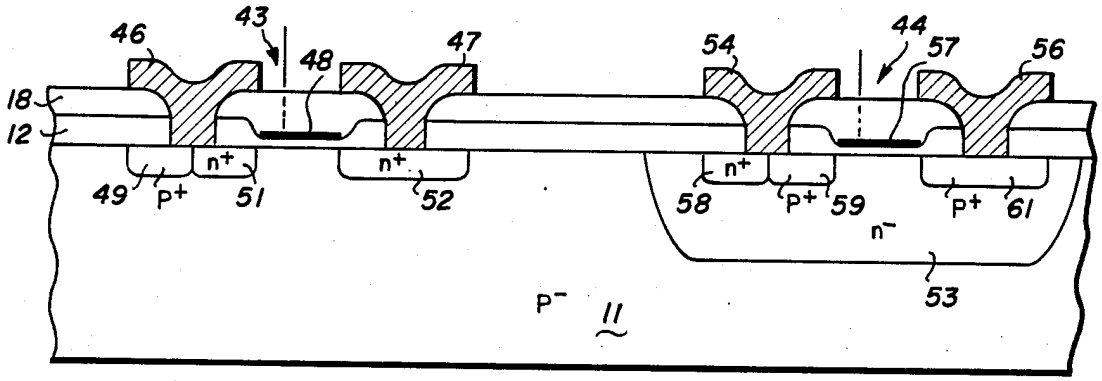

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Fig_4

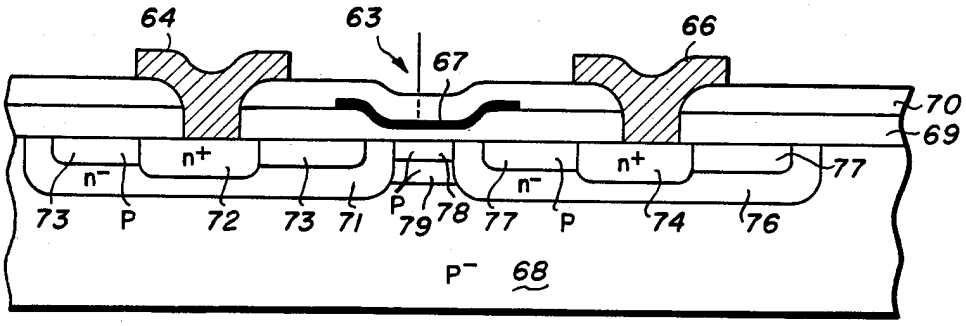
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Fig_5

# HIGH VOLTAGE MOS TRANSISTORS

## BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to high voltage metal-oxide semiconductor (MOS) transistors of the field-effect type. More specifically, the transistors can be made as either discrete or integrated devices of either n-channel or p-channel conductivity. The integrated devices can easily be combined with low voltage control logic on the same chip. Further devices of opposite conductivity can be combined in a complementary manner on the same chip.

2. Description of the Prior Art

Self isolation technology is used for making high voltage MOS devices, particularly integrated high voltage devices in combination with low voltage control logic on the same chip. The voltage is sustained by an offset gate, as a lightly doped extended drain region is used. Such devices can be considered as an IGFET or MOSFET in series with a single sided JFET. Two of such high voltage devices having opposite conductivity types can be used as a complementary pair on the same chip, with the device having an extended p-type drain being imbedded in an n-well in a p-substrate.

The voltage capability of such high voltage devices is determined by the doping of the substrate, the length of the extended drain region and the net number of charges therein. For optimum performance, the net number of charges should be around $1 \times 10^{12}/cm^2$. Such devices have been used for making display drivers in the one hundred to two hundred volt range, but the current capabilities of the devices are poor. The main advantage is that low voltage control logic easily can be combined on the same chip. For these devices, a general figure of merit can be determined by the product of $R_{on}xA$ (where $R_{on}$ is the on-resistance in the linear region and A is the area taken up by the device). For an n-channel device in the voltage range of two hundred fifty to three hundred volts, $R_{on}xA$ is typically 10–15 $\Omega$ mm$^2$. A discrete vertical D-MOS device in the same voltage range has a figure of merit of 3 $\Omega$ mm$^2$, but is much more difficult to combine with low voltage control logic on the same chip. Thus, the application of these high voltage devices is restricted to current level below 100 mA, such as display drivers. Even such drivers are more costly due to poor area efficiency of the high voltage devices.

## SUMMARY OF THE PRESENT INVENTION

An object of the present invention is to provide a more efficient high voltage MOS transistor.

Another object of the invention is to provide a high voltage MOS transistor that is compatible with five volt logic.

A further object of the invention is to provide a three hundred volt n-channel device with a figure of merit, $R_{on}$ x A, of about 2.0 $\Omega$ mm$^2$,

Briefly, the present invention includes an insulated gate, field-effect transistor (IGFET or MOSFET) and a double-sided junction gate field-effect transistor (JFET) connected in series on the same chip to form a high voltage MOS transistor. In a preferred embodiment of the invention, a complementary pair of such high voltage MOS transistors having opposite conductivity type are provided on the same chip.



Advantages of the invention include more efficient high voltage MOS transistors, compatibility with five volt logic, and for an n-channel device, voltage capability of three hundred volts with a figure of merit, $R_{on}$ x A, of about 2.0 $\Omega$ mm$^2$.

These and other objects and advantages of the present invention will no doubt become obvious to those of ordinary skill in the art after having read the following detailed description of the preferred embodiments which are illustrated in the various drawing figures.

## IN THE DRAWINGS

FIG. **1** is a diagrammatic view of a high voltage MOS transistor of the n-channel type embodying the present invention.

FIG. **2** is a diagrammatic view of a high voltage MOS transistor of the p-channel type embodying the present invention.

FIG. **3** is a diagrammatic view of the transistors shown in FIGS. **1** and **2** forming a complementary pair on the same chip.

FIG. **4** is a diagrammatic view of low voltage, C-MOS implemented devices that can be combined on the same chip with the complementary pair of high voltage MOS transistors shown in FIG. **3**.

FIG. **5** is a diagrammatic view of a symmetric high-voltage n-channel device wherein the source region and the drain region are similar.

## DESCRIPTION OF THE PREFERRED EMBODIMENT

Looking now at FIG. **1**, an n-channel type, high voltage MOS transistor, indicated generally by reference numeral **10**, is formed on a p-substrate **11** covered by a silicon dioxide layer **12**. A metal source contact **14** and a metal drain contact **16** extend through the silicon dioxide layer to the substrate. A polysilicon gate **17** is positioned between the source contact and the drain contact at a location where the silicon dioxide layer is very thin so that the gate is slightly offset and insulated from the substrate. The polysilicon gate is the gate electrode, and an insulation layer **18** covers the gate and the silicon dioxide layer.

Beneath the source contact **14**, a pocket **19** of $p^+$ material and a pocket **21** of $n^+$ material are diffused into the $p^-$ substrate **11**. The pocket **21** extends from beneath the source contact to the gate **17**. Beneath the gate is a threshold voltage implant **22** of p-type material for adjusting the threshold voltage and a punch through implant **23** of p-type material for avoiding punch through voltage breakdown. Beneath the drain contact **16**, a pocket **24** of $n^+$ material is diffused into the substrate. An extended drain region **26** of n-material is formed by diffusion or ion implantation on top of the p-substrate, and extends from beneath gate **17** to the pocket **24** and a similar distance to the opposite side of the pocket. A top layer **27** of p- material is provided by ion-implantation through the same mask window as the extended drain region to cover an intermediate portion thereof, while the end portions of the drain region are uncovered to contact the silicon dioxide layer **12**. The top layer is either connected to the substrate or left floating.

The gate **17** controls by field-effect the current flow thereunder laterally through the p-type material to the n-type material in the extended drain region **26**. Further flow through the extended drain region can be controlled by the substrate **11** and the top layer **27**, which

act as gates providing field-effects for pinching off the extended drain region therebetween. Thus, the transistor **10** can be considered as an insulated gate, field-effect transistor (IGFET or MOSFET) connected in series with a double-sided, junction-gate field-effect transistor (JFET). While the insulated gate, field-effect transistor shown is a conventional MOS type, it should be understood that it could also be a lateral D-MOS or a depletion MOS type.

By adding the top layer **27** over the extended drain region **26** and connecting this top layer to the substrate **11**, the net number of charges in the extended drain region can be increased from $1\times10^{12}/cm^2$ to around $2\times10^{12}/cm^2$, or approximately double. This drastically reduces the on-resistance of the transistor **10**. The pinch off voltage of the extended drain region can be reduced from typically around forty volts to below ten volts. Thus, a conventional short channel, thin gate oxide MOS transistors can be used as the series transistor instead of a D-MOS device. This results in the following benefits. First, the threshold voltage of a conventional MOS transistor is typically much lower than for a D-MOS device (0.7 volts compared to two four volts for the D-MOS device) and thus, is directly compatible with five volt logic. The D-MOS device usually requires an additional power supply of ten to fifteen volts for driving the gate. Second, the conventional MOS transistor has less on resistance and thus, further reduces the total on resistance.

As the p-type top layer **27** can be made very shallow with a depth of one micron or less, the doping density in that layer will be in the range of $5\times10^{16}$–$1\times10^{17}/cm^3$. At doping levels above $10^{16}/cm^3$, the mobility starts to degrade and a decrease in mobility will increase the critical electrical field for breakdown, thus giving a higher breakdown voltage for fixed geometry. The number of charges in the top layer is around $1\times10^{12}/cm^2$ and to first order approximation independent of depth.

The combined benefits of the above features result in a voltage capability of three hundred volts with a figure of merit, $R_{on}$ x A, of about 2.0 Ω $mm^2$ for the transistor **10**. Currently used integrated MOS transistors have a figure of merit of about 10–15 Ω $mm^2$, while the best discrete vertical D-MOS devices on the market in a similar voltage range have a figure of merit of 3–4 Ω $mm^2$.

With reference to FIG. **2**, a p-channel type, high voltage MOS transistor is indicated generally by reference numeral **30**. Since the layers of substrate, silicon dioxide, and insulation for this transistor are similar to those previously described for transistor **10**, they will be given like reference numerals. A p-substrate **11** is covered by a silicon dioxide layer **12** and an insulation layer **18**. A metal source contact **31** and a metal drain contact **32** extend through the insulation layer and the silicon dioxide layer to an n-well **33** that is embedded in the substrate. A polysilicon gate **34**, which is an electrode, is positioned between the source contact and the drain contact at a location where the silicon dioxide layer is very thin so that the gate is slightly offset and insulated from the n-well. The gate and the silicon dioxide layer are covered by the insulation layer **18**.

A pocket **35** of $n^+$ type material and a pocket **36** of $p^+$ type material are provided in the n-well **33** beneath the metal source contact **31**. The pocket **36** extends to the gate **34**. An extended drain region **37** of p-type material is formed in the n-well and extends from beneath the gate to a pocket **38** located beneath the drain contact **32**, and the extended drain region continues a similar distance on the opposite side of the drain contact. A top layer **39** of n-material is provided by ion-implantation through the same window of the mask as the extended drain region to cover an intermediate portion thereof. The end portions of the extended drain region are uncovered so as to contact the silicon dioxide layer **12**. The top layer is either connected to the n-well or left floating.

The gate **34** controls by field-effect the current flow thereunder laterally through the n-type material to the p-type material in the extended drain region **37**. Further flow through the extended drain region can be controlled by the n-well **33** and the top layer **39**, which act as gates providing field-effects for pinching off the extended drain region therebetween. Thus, the transistor **30** can be considered as an insulated-gate field-effect transistor (IGFET or MOSFET) connected in series with a double-sided, junction-gate field-effect transistor (JFET). The n-well under the extended drain region has to be depleted before breakdown occurs between the $p^+$ drain contact pocket **38** and the n-well.

Looking now at FIG. **3**, an n-channel transistor **10**, similar to that shown in FIG. **1**, and a p-channel transistor **30**, similar to that shown in FIG. **2**, are shown as a complementary pair on the same substrate **11** and isolated from each other. Since the details of each transistor has been previously described with reference to FIGS. **1** and **2**, no further description is considered necessary.

As shown in FIG. **4**, low voltage, C-MOS implemented devices **43** and **44** can be combined on the same p-substrate **11** as the high voltage devices **10** and **30**, shown in FIG. **3**. These low voltage devices enable low voltage logic and analog function to control the high voltage devices. The device **43** is an n-channel type having a source contact **46**, a drain contact **47** and a polysilicon gate **48**. A $p^+$ pocket **49** and an $n^+$ pocket **51** are provided in the $p^-$ substrate beneath the source contact. The $n^+$ pocket extends to beneath the gate. An $n^+$ pocket **52** is provided beneath the drain contact. The gate **48** is insulated from the substrate by the silicon dioxide layer **12**, but the gate controls the current flow through the substrate between pockets **51** and **52**. The gate is covered by the insulation layer **18**. An n-well **53** is provided in the substrate to accommodate the low voltage, p-channel device **44**. This device includes a source contact **54**, a drain contact **56** and a polysilicon gate **57**. An $n^+$ pocket **58** and a $p^+$ pocket **59** are provided in the n-well beneath the source contact and a $p^+$ pocket **61** is provided in the n-well beneath the drain contact. The gate **57** is insulated from the n-well and extends thereabove between pockets **59** and **61**.

It should be noted that the term "substrate" refers to the physical material on which a microcircuit is fabricated. If a transistor is fabricated on a well of n or p type material within a primary substrate of opposite type material, the well material can be considered a secondary substrate. Similarly, if a transistor is fabricated on an epitaxial layer or spi-island that merely supports and insulates the transistor, the epitaxial layer or epi-island can be considered a secondary substrate. An epi-island is a portion of an epitaxial layer of one conductivity type that is isolated from the remaining portion of the epitaxial layer by diffusion pockets of an opposite conductivity type. When complimentary transistors are formed on the same chip, the well in which one compli-

mentary transistor is embedded is formed by the same diffusion as the extended drain region for the other transistor.

FIG. 5 shows a symmetrical n-channel device 63 having a source contact 64 and a drain contact 66. A polysilicon gate 67 is insulated from a substrate 68 by a silicon dioxide layer 69 and the gate is covered by an insulation layer 20. An n-type extended source region 71 is provided beneath the source contact and an $n^+$ type pocket 72. A top layer 73 of p-type material is positioned over an intermediate portion of the extended source region, while the end portions of the extended source region contact the silicon dixode layer thereabove. Beneath the drain contact is an $n^+$ type pocket 74 and an n-type extended drain region 76. A top layer 73 of p-type material is positioned over an intermediate portion of the extended drain region and end portions of the extended drain region contact the silicon dioxide layer. An implant 78 of the p-type material is provided under the gate 67 between the extended source region and the extended drain region for sustaining the threshold voltage. A similar implant 79 for sustaining the punch-through voltage is provided beneath the implant 78. Since the symmetrical channel device has both an extended source an an extended drain, the source can sustain the same high potential as the drain. A symmetric p-channel device could be made in a similar way using opposite conductivity type materials.

From the foregoing description, it will be seen that an efficient, high voltage MOS transistor has been provided. This transistor is compatible with five volt logic which easily can be integrated on the same chip. The transistor has a voltage capability of three hundred volts for an n-channel device, and has a figure of merit, $R_{on} \times A$, of about 2.0 $\Omega mm^2$. The transistor is formed by an insulated-gate field-effect transistor and a double-sided junction-gate field-effect transistor connected in series on the same chip. These transistors can be made as either discrete devices or integrated devices of either n-channel or p-channel conductivity. The integrated devices can be easily combined with low voltage control logic on the same chip. Further devices of opposite conductivity can be combined in a complementary manner on the same chip.

Although the present invention has been described in terms of the presently preferred embodiment, it is to be understood that such disclosure is not to be interpreted as limiting. Various alterations and modifications will no doubt become apparent to those of ordinary skill in the art after having read the above disclosure. Accordingly, it is intended that the appended claims be interpreted as covering all alterations and modifications as fall within the true spirit and scope of the invention.

I claim:

1. A high voltage MOS transistor comprising:
- a semiconductor substrate of a first conductivity type having a surface
- a pair of laterally spaced pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,
- a source contact connected to one pocket,
- a drain contact connected to the other pocket,
- an extended drain region of the second conductivity type extending laterally each way from the drain contact pocket to surface-adjoining positions,
- a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjoining positions,
- said top layer of material and said substrate being subject to application of a reverse-bias voltage,
- an insulating layer on the surface of the substrate and covering at least that portion between the source contact pocket and the nearest surface-adjoining position of the extended drain region, and
- a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the source contact pocket and the nearest surface-adjoining position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.

2. The high-voltage MOS transistor of claim 1 wherein,

said top layer has a depth of one micron or less.

3. The high-voltage MOS transistor of claim 1 wherein,

said top layer has a doping density higher than $5 \times 10^{16}/cm^3$ so that the mobility starts to degrade.

4. The high voltage MOS transistor of claim 1 having one channel conductivity type in combination with a complementary high voltage MOS transistor of an opposite channel conductivity type combined on the same chip and isolated from each other.

5. The high voltage MOS transistor of claim 1 combined on the same chip with a low voltage CMOS implemented device.

6. The combination of claim 5 further including,
- a complementary high voltage MOS transistor, and
- a complementary low voltage CMOS implemented device on the same chip and isolated from each other.

7. A high voltage MOS transistor comprising:
- a semiconductor substrate of a first conductivity type having a surface,
- a pair of laterally spaced pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,
- a source contact connected to one pocket,
- an extended source region of the second conductivity type extending laterally each way from the source contact pocket to surface-adjoining positions,
- a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended source region between the surface-adjoining positions,
- said top layer and said substrate being subject to application of a reverse-bias voltage,
- a drain contact connected to the other pocket,
- an extended drain region of the second conductivity type extending laterally each way from the drain contact pocket to surface-adjoining positions,
- a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjoining positions,
- said top layer of material and said substrate being subject to application of a reverse-bias voltage,
- an insulating layer on the surface of the substrate and covering at least that portion between the nearest surface-adjoining positions of the extended source region and the extended drain region, and
- a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the nearest surface-adjoining positions of the extended source region and the extended drain region, said gate electrode controlling by field-effect the current flow thereunder through the channel.

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Appendix 1 – Side-by-side comparison of the ’719 and ’075 patents.

’719 Patent claim 8

8. A high voltage MOS transistor comprising:
a semiconductor substrate of a first conductivity type having a surface,
a pair of laterally spaced source and drain pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,
an extended drain region of the second conductivity type extending laterally each way from said drain pocket to surface-adjoining positions,
a surface adjoining, top layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain pocket and the surface-adjoining positions,
said top layer of material and said substrate being subject to application of a reverse-bias voltage,
an insulating layer on the surface of the substrate and covering at least that portion between the source pocket and the nearest surface-adjoining position of the extended drain region, and
a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the source pocket and the nearest surface-adjoining position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.

’075 Patent claim 1

1. A high voltage MOS transistor comprising:
a semiconductor substrate of a first conductivity type having a surface
a pair of laterally spaced pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,
a source contact connected to one pocket,
a drain contact connected to the other pocket,
an extended drain region of the second conductivity type extending laterally each way from the drain contact pocket to surface-adjoining positions,
a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjoining positions,
said top layer of material and said substrate being subject to application of a reverse-bias voltage,
an insulating layer on the surface of the substrate and covering at least that portion between the source contact pocket and the nearest surface-adjoining position of the extended drain region, and
a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the source contact pocket and the nearest surface-adjoining position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.

**UNITED STATES DISTRICT COURT**
**FOR THE EASTERN DISTRICT OF TEXAS**
**MARSHALL DIVISION**

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|---|---|
| **FAIRCHILD SEMICONDUCTOR CORPORATION, a Delaware corporation, and INTERSIL CORPORATION, a Delaware corporation,**<br><br>**Plaintiffs,**<br><br>**v.**<br><br>**POWER INTEGRATIONS, INC., a Delaware corporation,**<br><br>**Defendants.** | **C.A. No. 2:06-CV-151 (TJW)** |

**ORDER GRANTING POWER INTEGRATIONS' MOTION TO DISMISS**

ON THIS DAY, came on to be considered Power Integrations, Inc.'s Motion to Dismiss, or in the Alternative, to Transfer This Case to Delaware in the above-styled and numbered cause. After considering said motion, the Court is of the opinion that said motion should be GRANTED, and that all matters in this suit against Power Integrations, Inc. are dismissed with prejudice.